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Device characteristics of amorphous indium-gallium-zinc-oxide channel capped with silicon oxide passivation layers

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ABSTRACT

It was investigated how the amorphous indium-gallium-zinc-oxide (a-IGZO) channel of a back-gate of thin film transistor (TFT) is affected by the deposition of silicon oxide layers on their top surfaces by radio frequency magnetron sputtering. Preliminary investigations showed that the deposition of silicon oxide layer caused damages to the surfaces of pristine silicon wafers resulting in substantial roughening. However, bombardments by the energetic particles involved in the sputtering process seem to have played beneficial roles in that the a-IGZO channel TFTs showed improved performances in respect of the carrier density, field effect mobility, and on-off current ratio. Such improvements are attributed to the modification of the a-IGZO channel to decrease the concentration of oxygen vacancy sites and/or to average the oxygen vacancy sites thereby increasing the carrier concentrations and decreasing the density of trap sites, as revealed in the negative shift of the threshold voltage. On the other hand, such channel modification by the passivation process resulted in the slight increase in the subthreshold swing. It is suggested that the a-IGZO channel TFTs can be passivated by simple sputtering process without etch stop layer since the process rather improved the device performances despite some damages to the passivated surfaces.

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1. Introduction

Amorphous semiconductors are widely used in large-area electronic devices, such as flat panel displays and photovoltaic cells, where cost and low-temperature processability are of primary concerns. Hydrogenated amorphous silicon (a–Si:H) has been the major material for such applications to date. Recent advances in optoelectronic devices necessitated the search for alternatives to a–Si: H due to its limited physical properties such as opacity, brittleness, and rigidity. One promising candidate is amorphous indium-gallium-zinc-oxide (a–IGZO) which has the superior field effect mobility higher than 10 $\text{cm}^2\text{/Vs}$ compared to those in the range of 1 cm²/Vs of typical a-Si:H $[1]$. Further advantages of a–IGZO include low-temperature processability including room temperature, transparency to visible light, mechanical flexibility on bending, etc. $[2,3]$. On the other hand, a -IGZO is vulnerable to ambient oxygen, hydrogen or moisture which degrades the device performance. Therefore, suitable passivation

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<http://dx.doi.org/10.1016/j.mssp.2016.03.020> 1369-8001/& 2016 Elsevier Ltd. All rights reserved. layer should be added to the a–IGZO channel for protection when thin film transistors (TFTs) are fabricated [\[4,5\]](#page--1-0).

One possible means of the protection is to apply organic passivation layer which has the advantages of low cost and flexibility $[6]$. However, organic layers are prone to degradation and damage especially during additional device processes. Inorganic material such as silicon oxide can be used as passivation layer instead which have improved environmental stability than polymers. Silicon oxide passivation layers can be deposited by variety of techniques including electron beam (e-beam) evaporation, plasma-enhanced chemical vapor deposition, and sputtering [\[7,8\].](#page--1-0) Among these, radio frequency (RF) magnetron sputtering enables low-cost and lowtemperature deposition in large area. In this case, however, the lowtemperature thin film deposition technique involves plasma and particles of depositing material which bombard the top surface of the a–IGZO channel with kinetic energies during the deposition of the "protective" passivation layer causing some damages. This damage can be avoided by introducing etch stop layer (ESL) on the channel layer [\[9\],](#page--1-0) but it causes resistance capacitance delay while increasing the complexity of device process. If the ESL-free device structure is to be adopted with the low-cost and low-temperature process for the deposition of the passivation layer, it is necessary to understand how the introduction of the passivation layer by RF

magnetron sputtering affects the channel characteristics and resulting device performances.

Existing works on the effect of plasma treatments on the device performances have treated the treatment as a passivation process itself. Although the plasma treatment can have some passivation effect on the channel layer, deposition of the passivation layer inevitably bombards the channel surface with incoming particles. This study, therefore, aims at the understanding of the relation between the process parameters and the characteristics of the a– IGZO channel TFTs to establish the ESL-free deposition of silicon oxide passivation layer by RF magnetron sputtering.

2. Experimental procedure

The a–IGZO channel TFTs were prepared in a back-gated configuration as schematically illustrated in Fig. 1 where the channel width and length were 1000 and $200 \mu m$, respectively. Initially, 30-nm-thick a -IGZO channel layers were deposited on an SiO₂ $/p^{++}$ Si substrate by DC magnetron sputtering using an IGZO target (InO₃:Ga₂O₃:ZnO=1:1:1 mol%). The dielectric layer on the substrate was introduced by thermal oxidation to the thickness of 300 nm. The deposition was carried out in $Ar/O₂$ mixture (10 vol% $O₂$) at the working pressure of 5 mTorr with the sputtering power of 150 W at room temperature. The as-deposited a– IZGO films were annealed in air at 300 °C for 1 h. Source and drain electrodes were prepared subsequently by e-beam evaporation of Al. In order to investigate the effect of the passivation layer addition, 30 nm-thick silicon oxide layer was attached on the top surface of the device structure by RF magnetron sputtering with the sputtering power of 100, 200, and 300 W at room temperature. For the deposition $Ar/O₂(1:1)$ mixture gas was introduced into the chamber at the working pressure of 15 mTorr. For comparison, another device was prepared by adding the silicon oxide layer by e-beam evaporation. A reference device was prepared where no protection layer was added. The device characteristics were estimated using a semiconductor parameter analyzer (Agilent B1500A, Agilent Technologies).

Damaging effects of the passivation processes were separately investigated by depositing the silicon oxide layer on pristine ptype Si (100) wafer surfaces by the same methods as used to passivate the TFTs. At first, native oxides on the p-type Si wafers were eliminated by HF solution and rinsed in deionized water. Then, 30-nm-thick silicon oxide layer was deposited on the top surface of the device structure by RF magnetron sputtering with the power of 100, 200, 300 W. Another sample was prepared by adding the silicon oxide layer by e-beam evaporation. After deposition, the silicon oxide layers were removed using 1% HF solution for 20 s to expose the interface between the passivation layer and the wafer. Damages on these surfaces (layer/wafer interfaces) were evaluated by measuring the contact angle using a contact angle analyzer (KSV, CAM 100) and the surface roughness using an atomic fore microscope (AFM, Park System, XE-100).

Fig. 1. Schematic showing the configuration of the back-gated a-IGZO channel TFT with silicon oxide passivation capping considered in this study.

3. Results and discussion

The immediate effect of the bombardment by the depositing particles on the channel surface would be its physical damage [\[10\].](#page--1-0) It was first investigated how the passivation process have affected the sample surfaces by depositing silicon oxide layer on a p -Si wafer and wet etching with 10:1 buffered oxide etchant before the application of various process parameters for the deposition of the silicon oxide passivation layer on the $a - IGZO$ channel. [Fig. 2](#page--1-0) (a) shows the degree of surface modification in respect of the contact angle. The contact angle of the pristine p-Si wafer was 83.2° initially. When the silicon oxide layer was deposited by e-beam evaporation, the angle decreased to 81.9°. Once the RF magnetron sputtering was used for the deposition, the angles decreased to 80.5, 73.6, and 66.1° as the plasma powers of 100, 200, and 300 W were applied, respectively. Lower contact angle indicates higher surface energy [\[11\]](#page--1-0). Unless there are changes in the chemical states of the surface atoms, changes in surface energy can be associated with the increased number of broken bonds of the surface atoms, which would be achieved by the increased surface area by roughening [\[12\].](#page--1-0) These results suggest that addition of the silicon oxide protective layer indeed caused some damages to the surface and that the RF magnetron sputtering was more damaging than the e-beam process [\[13\]](#page--1-0). The actual surface damage was visualized using AFM. Fig. $2(b)$ shows the surface morphology and RMS roughness which is well correlated to the contact angle results in [Fig. 2\(](#page--1-0)a) $[14]$. It can be seen that rougher surfaces resulted as the RF magnetron sputtering was applied to deposit silicon oxide layer while the roughness increases with higher plasma power.

The introduction of the silicon oxide layer on a pristine $p-Si$ wafer caused some damages on the wafer surface as shown above. The same would be the case when the silicon oxide layer is deposited as protective layer on the top surface of the $a -$ IGZO channel of the device. In addition, it is expected that the channel layer itself would undergo some microstructural changes under the influence of the $Ar/O₂$ plasma and the impinging particles since the channel thickness of the TFT samples in this study is only 30 nm. An immediate consequence of this would be changes in the device operation characteristics. [Fig. 3](#page--1-0) shows the output characteristics of the a-IGZO channel TFTs having silicone oxide protective layers deposited by RF magnetron sputtering and e-beam evaporation. Also shown is the transfer curve for the TFT without the protective layer (reference device) for comparison. It is seen in [Fig. 3](#page--1-0) that the drain current, I_d , increased significantly when the silicon oxide layer was added by sputtering and that the current increased further with higher sputtering power. This increase in the I_d implies the increase in the channel conductance which could be achieved by higher carrier concentration and mobility [\[15\].](#page--1-0) Therefore, it is presumed that the deposition of the silicon oxide layer on the top surface of the a-IGZO channel by RF magnetron sputtering with $Ar/O₂$ plasma have modified the channel properties microscopically as well.

Microscopic changes in the channel properties by the passivation process can further be seen in the transfer characteristics shown in [Fig. 4](#page--1-0) and [Table 1.](#page--1-0) First, there is a negative shift in the threshold voltage (V_{th}) , with the addition of the protective layer by sputtering $[16]$. The V_{th} of the reference device, where no protective layer was added, was initially almost 0 V. When the protective layer was added by e-beam evaporation, there was practically no change in the V_{th} . On the other hand, when the layer was added by sputtering, the V_{th} shifted to -1.409 V and -4.861 V at the sputtering power of 100 W and 200 W, respectively. With higher sputtering power of 300 W, V_{th} could not be measured since the device was always in the "on" state regardless of the gate voltage,

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