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Numerical simulation of lateral diffused metal oxide semiconductor field effect transistors: A novel technique for electric field control to improve breakdown voltage

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ABSTRACT

In this paper, we propose a novel technique to control the electric field in Lateral Diffused Metal Oxide Semiconductor (LDMOS) Field Effect Transistors, in order to increase the breakdown voltage. The key idea in this work is increasing the smoothness of the electric field by extra oxide (EO) on the gate sidewall at the drain side of a deep gate structure. The EO region effects on the breakdown voltage by uniformity of the electric field profile. Our results show that the electric field will be maximally flatted by optimization of EO region. Therefore, the proposed structure is called maximally flat deep gate LDMOS (MFDG-LDMOS). The novel features of MFDG-LDMOS are simulated and compared with a conventional LDMOS (C-LDMOS). Our results show that the breakdown voltage and the on-state resistance of the MFDG-LDMOS improve about 48% and 25% in comparison with the C-LDMOS, respectively.

1. Introduction

High performance power transistors are essential for integrated circuits and discrete power devices. Among different power transistors, Lateral Double Diffused MOSFET (LDMOS) structures have been widely used in intelligent power applications [1,2]. The advantages of these devices over traditional vertical double-diffused MOSFETs include the reduction of the number of fabrication steps, multiple output capability on the same chip, and compatibility with advanced VLSI technologies. LDMOSFETs with VLSI processes make the prospect of intelligent power ICs a reality. However, low breakdown voltage in LDMOSFET devices is the major problem that restricts power applications. In order to increase breakdown voltage, various structures have been proposed to improve the performance of the LDMOSFETs [3–5]. In addition, both low on-state resistance and high breakdown voltage are considered as prime parameters of power devices. However, simultaneously obtaining the desired characteristic for both parameters cannot be possible in the conventional structures. In fact, most of the time improvement in one parameter will degrade the characteristic of another parameter.

In this paper, we present a novel technique to control the electric field in LDMOSFETs for improving the breakdown voltage. The key idea in our work is increasing the smoothness of the electric field by extra oxide (EO) on the gate side wall at the drain side of a deep gate structure. So, the proposed structure is called maximally flat deep gate LDMOS (MFDG-LDMOS). In the MFDG-LDMOS, by locating the EO region in the gate side wall, the electric field at the junction of drift region and the gate will be smoother and therefore the breakdown voltage increases [6–9]. The proposed structure is simulated by two dimensional ATLAS simulator [10]. By optimization of EO region, we have shown that the electric field will be maximally flatted and

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therefore the maximum breakdown voltage is achieved. The proper breakdown voltage and on-state resistance can be mentioned as the main approaches of this device. Our results show the breakdown voltage increases as expected in comparison with a conventional LDMOS (C-LDMOS) and the DPG structure without the EO region (CDG-LDMOS).

2. Device structure and simulation

The schematic cross section of MFDG-LDMOS is illustrated in Fig. 1. As the figure shows, an extra oxide region has been located at the gate sidewall on the drain side of the deep gate structure. The length and depth of EO region are named L_{EO} and D_{EO}, respectively as shown in Fig. 1. The main parameters of the proposed structure are mentioned in Table 1.

In two dimensional numerical simulations, beside the Poisson and drift/diffusion equations, Schockly–Read–Hall (SRH) and Auger models are considered for generation/recombination [11]. Klassen's model is used to account for lattice scattering, impurity scattering, carrier-carrier scattering and impurity clustering effects at high concentration due to the utilization of SOI (silicon on insulator) structure [12].

It is worth noting that the two dimensional (2D) simulator is calibrated with experimental data [13]. The transfer characteristics at the drain bias of 0.1 V of SOI-LDMOS are extracted from experimentally measured have been compared with ATLAS simulation in Fig. 2 [13].

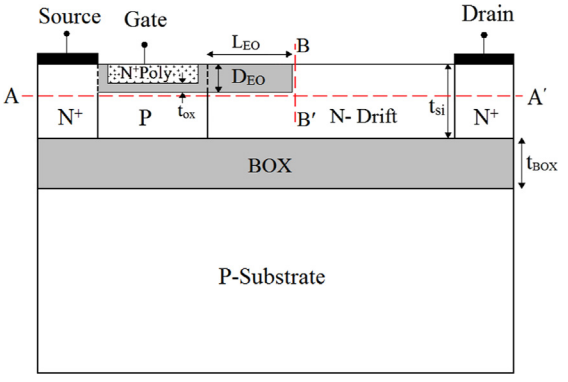

Fig. 1. Schematic of maximally flat deep gate of LDMOS (MFDG-LDMOS).

According to the figure a good agreement is obtained by comparing 2D simulated and experimental data.

A process flow has been proposed for the fabrication of the MFDG-LDMOS device. As shown in Fig. 3(a), the starting material is a p-type 100-oriented silicon wafer. To begin with, we should create a SiO_2 layer in the 1.5 μm depth. This SiO_2 layer can be created with the separation by implementation of the oxygen (SIMOX) method [14]. The thickness of the SiO_2 layer is 1 μm. The next process, which is shown in Fig. 3(d), is another ion implantation (by SIMOX process) to create the gate oxide. As a result, the window is created and filled with silicon, and the other region is filled by SiO_2 shown in Fig. 3(e). In the next step, ion implantation is used to create the extra oxide. Finally, thermal annealing is used to reduce traps and have better crystalline silicon to create source, drain, channel, and drift regions. It is important to note that the fabrication process is simple and only one extra mask is needed.

3. Results and discussion

The increase of breakdown voltage can be the result of a new peak in the electric field. This new peak, which is generated due to situating the EO region at the interface of deep gate and drift region, effects on the smoothness of the

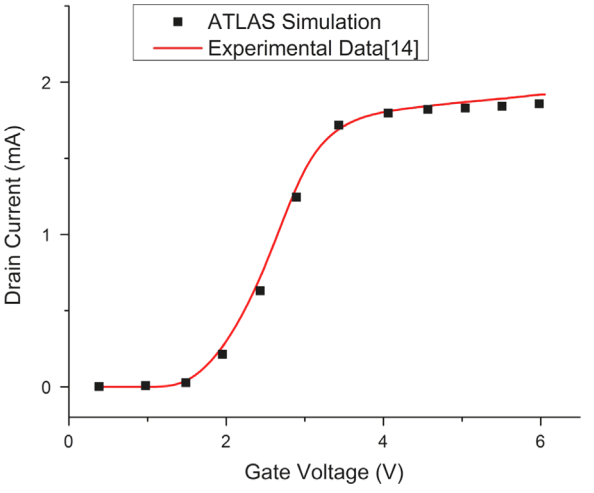

Fig. 2. The output characteristic of simulated SOI-LDMOS has been compared with experimental results in Ref. [13] at the drain bias of 0.1 V.

Table 1
Required characteristics for designing the MFDG-LDMOS, CDG-LDMOS, and C-LDMOS structures.

Device parameters	MFDG-LDMOS	CDG-LDMOS	C-LDMOS
Channel length	2 μm	2 μm	2 μm
Drift region length	6 μm	6 μm	6 μm
Extra oxide length (L_{EO})	3 μm	Not defined	Not defined
Extra oxide depth (D_{EO})	0.5 μm	0.5 μm	Not defined
Buried oxide thickness(t_{BOX})	1 μm	1 μm	1 μm
Silicon thickness(t_{Si})	1.5 μm	1.5 μm	1.5 μm
Gate oxide thickness(t_{ox})	50 nm	50 nm	50 nm
Channel doping density	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
Source/drain doping density	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Substrate doping density	5×10^{13} cm^{-3}	5×10^{13} cm^{-3}	5×10^{13} cm^{-3}
Drift region doping density	5×10^{15} cm^{-3}	5×10^{15} cm^{-3}	5×10^{15} cm^{-3}