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Effects of post-lift-off annealing conditions on contact oxidation of Ti–Au top-contacts in In-Sn–Zn–O TFT

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ABSTRACT

Thin film transistors (TFT) with an indium based mixed oxide semiconductor are investigated for titanium–gold top-contacts. It is noticed that upon post annealing, in order to remove chemical residuals from top-contact lift-off steps, oxidation of titanium occurs depending on the annealing conditions. Mobility of the TFT is strongly affected by contact oxidation arising from this post lift-off annealing process. Oxidation of the top-contact is facilitated by adsorbed surface oxygen or out-diffusing oxygen from the semiconductor depending on the post lift-off annealing conditions. A passivation layer that binds effectively to surface vacancies and removes adsorbed oxygen species from the semiconductor surface is demonstrated. The combinations of this passivation layer with relatively low temperature and short post lift-off annealing in an oxygen deficient environment result in significantly reduced contact oxidation and subsequently better transistor performance. Contact resistance as low as 90 Ω cm and mobility as high as 5.3 $cm^2/V\,s$ are obtained for solution processed mixed metal oxide semiconductor in top-contact geometry.

1. Introduction

Indium based solution processed metal oxide semiconductors have garnered a lot of interest in recent years due to their tremendous ability to retain high mobility even in amorphous solution processed forms, enabling printable roll-to-roll fabrication for display backplanes [1–4]. Mixed metal oxide semiconductors based on indium, like indium gallium zinc oxide (IGZO), have overcome one of the degradation problems of indium-only oxide semiconductors by careful selection of component metals that bind relatively strongly to the oxygen and thereby suppressing oxygen vacancies formation [2,5]. This decreases the mobility of the semiconducting layer to some extent; however the stability achieved by stronger metal oxide bonds and the uniformity achieved by amorphization due to aliovalent component metals outweigh the loss in mobility [5,2] The recently reported mobility calculated from gradual channel approximation of 10–20 $cm^2/V\,s$ [3] for sol–gel based IGZO is more than sufficient for flexible display applications in comparison to all amorphous silicon or organic semiconductor based TFTs [3,6]. This combination of high mobility and uniformity in printable form is steering the display industry towards the next generation of large-area and foldable displays. One of the challenges hindering progress is the choice of contact metal in top-contact geometry where low work function metals, which are expected to form ohmic contact with wide band gap semiconductors, tend to oxidize due to the out-diffusion of oxygen from the semiconductor upon

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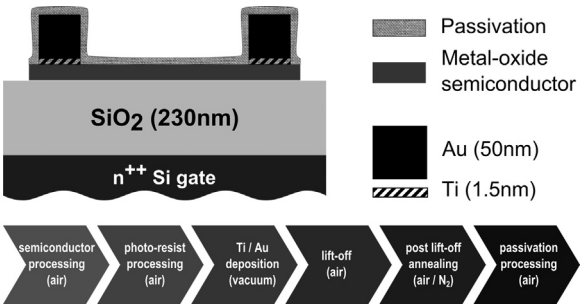

Fig. 1. Schematic (not to scale) and process flow of the investigated bottom gate top contact thin film transistors.

annealing [7,8]. The resulting contact resistance prevents the device from operating at the semiconductor inherent field effect channel mobility, significantly lowering the device's electrical performance. Shimura et al. have shown that low work function metals such as titanium and silver form ohmic contact and achieve lower specific contact resistance than higher work function metals such as gold or platinum which show non-ohmic contact behavior in IGZO based TFTs [7]. However, low work function metals are extremely sensitive to fabrication processes and exhibit large distribution in specific contact resistance, larger values of which are comparable to their non-ohmic counterparts [7]. This paper introduces a novel method of overcoming this problem by carefully selecting an optimized post metal deposition annealing condition and an effective passivation layer.

2. Experimental

2.1. Device architecture and materials

The transistors are fabricated in bottom-gate top-contact (BGTC) configurations as shown schematically in Fig. 1. A highly doped silicon wafer with thermally grown silicon oxide layer of 230 nm comprises the gate electrode and gate dielectric respectively. Metal oxide precursor, iXsenic® S, a product of Evonik Industries AG, is spin coated and annealed at 350 °C to form the final 8 nm thick layer of indium tin zinc oxide (In–Sn–Zn–O) based semiconductor layer. A 1.5 nm of titanium (Ti) followed by 50 nm of gold (Au) is deposited by e-beam evaporation and patterned by photolithography and lift-off process to define the top-contacts. The devices are then (post lift-off) annealed quickly at different temperatures and environments to remove residual solvents introduced during the top-contact patterning steps. A very wide band gap metal oxide based insulating precursor, iXsenic® P1207, a product of Evonik Industries AG, is then spin coated and annealed at 350 °C in air for half an hour to form the 2–3 nm thick passivation layer on the semiconductor surface. The passivation is a single component highly stable metal oxide and is deposited on the semiconductor surface to avoid instability caused by surface defects [9]. Lastly, the semiconductor together with passivation is patterned by etching with oxalic acid so that it effectively covers only the channel region. This is necessary to prevent leakage current due to the semiconductor intrinsic conductivity. This paper discusses how crucial the annealing step introduced after the lift-off process and before the passivation is, here referred to as post-lift-off (PLO) step, on the device performance.

The trends in the experiments shown in this paper are reproduced 3 times. Due to possible scattering resulting from statistical deviations between different batches, results from one batch is shown in this paper.

2.2. Measurement techniques and data analysis

The current–voltage characteristics of the transistors are measured in a probe station coupled with precision semiconductor parameter analyzer Agilent 4156C. The transistors are fabricated with channel lengths (L) ranging from 10 μm to 50 μm whereas the channel width (W) is kept constant at 2000 μm for all devices. The transfer curves are all measured at drain-source voltage of $V_{DS} = 2\ V$ to avoid current crowding at larger drain fields.

Mobility (μ) and the channel disorder parameter γ is extracted using the Vissenberg-Matters model for highly disordered system [10]. In this model, charge transport is assumed to occur through variable range hopping between localized states in the tail of an exponential density of states. Mobility is hence dependent on the charge carrier density in the channel which in turn is dependent on the effective gate voltage–gate voltage minus the threshold voltage, normalized to the μ_0 reference voltage, V_{aa}. The parameter γ and V_{aa} have been explained in detail by Gburek and Wagner [11]. The relation between $\mu, \mu_0,\ \gamma$ and V_{aa} is shown as,

$$\mu = \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{aa}} \right)^{\gamma} \quad (1)$$

μ_0 is the mobility at $V_{aa} = V_{GS} - V_{th}$ and V_{GS} and V_{th} are the applied gate voltage and measured threshold voltage respectively. The constant $V_{aa} = 50$ V is chosen for all transfer curve fits. This allows mobility for all PLO annealing scenarios to be compared at the same induced carrier concentration in the linear regime.

Width normalized contact resistance R_CW and channel resistance R_{ch} per unit channel area is extracted using the conventional Transmission Line Method (TLM) [12]. The plot of the product of the total resistance R_T and W versus L should result in a linear dependence as shown in Eq. (2) if the channel is uniform and the transistor is working in the linear regime. The y-intercept of the linear fit would then give the total width normalized contact resistance R_CW and the slope would give the channel resistance R_{ch} per unit area.

$$R_T \mathrm{W} = R_C \mathrm{W} + R_{ch} L \quad (2)$$

Surface oxygen composition of the semiconductor layer with and without passivation is compared using x-ray photoelectron spectroscopy (XPS) using Mg k-alpha excitation source. The semiconductor layers for XPS measurements are deposited directly on highly doped Si wafer without a thermally grown oxide layer to avoid charging effects during the measurements. The peaks obtained are fitted keeping the full width half maximum (FWHM) constant between component peaks.