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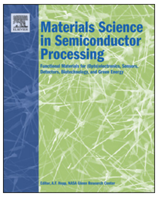

Temperature bistability in a silicon wafer with a doped layer on lamp-based heating

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ABSTRACT

The effect of a heavily doped layer formed at the surface of a lightly doped silicon wafer upon the transfer characteristic of the entire heat system involving the wafer, lamp heater, and cooling system is simulated. The layer parameters that provide the hysteresis-loop-shaped transfer characteristic are determined. The dependence of the integrated emissivity of the silicon wafer with a doped layer on the layer thickness, doping level, and position with respect to the radiation source is analyzed. It is shown that, in the temperature region of semitransparency of the silicon wafer, there exists some critical layer thickness such that the integrated emissivities of both sides of the wafer are equal. It is found that the parameters of the hysteresis loop depend on the layer position with respect to the radiation source. The expression for the layer-related correction to the temperature of the wafer when subjected to thermal processing in a lamp reactor with supplementary heat removal by convection or heat conduction is derived.

1. Introduction

Rapid thermal processing of semiconductor materials is extensively used in the production of low-power integrated circuits (ICs), ICs for high-power electronics, nano- and micro-scaled electromechanical systems (MEMS), optical and optoelectronic devices, planar displays, solar cells, and compound-semiconductor-based ICs as well as in advanced technologies [1,2]. Controversial constraints often placed on the temperature conditions of thermal processing in the production of nano- and micro-scaled devices, such as, e.g., the need for a high level of activation of dopant impurities in combination with the minimum possible spreading of the initial doping profile on post-implantation annealing stimulate the search for new approaches to the solution of technological problems [3]. One of such approaches is based on the use of spike [4] or flash [5] annealing processes. The distinctive feature of these modifications of annealing is the time limitations imposed on the dopant diffusion process at high peak temperatures and on the temperature rise and decay rates. This is especially true for flash annealing [5,6] that can be considered as a thermal process intermediate in character between rapid lamp annealing and laser treatment of the semiconductor wafer surface [7]. Both on laser treatment and flash annealing, a high-power radiation pulse with the duration shorter than the thermal response time of the wafer produces a heated surface region, whose temperature is much higher than the temperature of the underlying part of the wafer. This means that the time limitations imposed on the duration of annealing by the incident high-power radiation flux provide conditions for spatial confinement of the diffusion zone in the wafer. However, the diffusion zone can be spatially confined even without any limitations on the time of thermal processing of the semiconductor wafer. The effects of this type were studied by analyzing the interaction of laser radiation with semiconductor samples and are currently known as lateral and longitudinal optical bistabilities upon saturating absorption [8,9]. In the case of lateral bistability, at the semiconductor surface, there simultaneously exist high- and low-temperature regions [8] corresponding to the upper and lower branches of the

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hysteresis loop that describes the dependence of the sample surface temperature on the incident radiation intensity. In the case of longitudinal bistability, the high-temperature region is localized within the wafer and can either reside near the wafer surface or move back and forth along the radiation propagation direction, depending on the parameters of the incident radiation beam and the properties of the absorbing medium [8–10]. The temperature bistability phenomenon upon increasing absorption and the related effects can occur not only on the interaction of semiconductor samples with laser radiation, but also on irradiation of semiconductor wafers in the process of infrared (IR) lamp heating in rapid thermal processing (RTP) setups. The possibility of temperature bistability in a silicon wafer on heating and cooling in the thermal reactor of an RTP setup is shown theoretically and experimentally [11]. It is also shown that, under certain conditions of heat treatment of a silicon wafer in an RTP setup, the wafer can exhibit temperature oscillations [12]; i.e., under the RTP conditions, a silicon wafer can exhibit triggering and oscillatory temperature regimes typical of the unstable behavior of dynamical systems [13]. The possibility of the bistable behavior depends on the conditions of heat exchange between the silicon wafer and the elements of the working thermal reactor as well as on the optical and electrical properties of the wafer on its own. It is shown that the bistability appears under supplementary conductive or convective heat removal from the wafer and heavily depends on the doping level of the wafer [11,14]. According to Rudakov et al. [11] and Ovcharov et al. [14], the temperature bistability phenomenon in a silicon wafer in a water-cooled thermal reactor can be observed at low *n*- or *p*-type dopant concentrations up to $\sim 2 \times 10^{17}$ cm^{-3} [14]. To observe the temperature bistability effect in a heavily doped silicon wafer, one needs specially designed reactors that operate at low temperatures of the cooling agent and, thus, provide conductive and convective heat removal from the wafer.

The correlation of the temperature bistability effect with the impurity concentration in a uniformly doped silicon wafer naturally raises the question of whether the effect occurs in a wafer with a nonuniform distribution of impurities. Specifically, the question arises of how doped layers or, more generally, film structures (e.g., silicon-on-insulator (SOI) structures or multilayered gate structures) influence the temperature bistability effect in such a wafer. In this context, the purpose of this study is to clarify the issues concerned with the strength of the temperature bistability effect in a silicon wafer at different parameters of the layers and films formed at the wafer surface and to analyze the possibilities of strengthening or, on the contrary, weakening the bistability effect in accordance with the specified technological problems to be solved.

2. The model and basic equations

Let us consider a standard silicon wafer mounted in a lamp heating reactor, in which heat is removed from the wafer via the combined processes, specifically, either by emission and heat conduction or by emission and convection. In the former case, the wafer is mounted above the water-cooled pedestal, and supplementary heat removal occurs through the gas-filled gap between the wafer and the pedestal. In the latter case, supplementary heat removal is carried out by the gas flow blowing the wafer. Such a reactor can be simulated as a radiation-closed heat system involving three semiinfinite plane-parallel isothermal plates: a plate (heater) simulating the set of tungsten halogen incandescent-filament lamps, a working silicon plate serving as the sample (wafer) to be studied, and a pedestal-simulating plate (absorber) that absorbs incident radiation and possesses material properties close to those of a blackbody (BB). The model of such heat system, in which heat is removed from the wafer by the combined mechanism of emission and thermal conduction/convection, is schematically shown in Fig. 1. For a wafer in such heat system, the heat balance equation is [11]

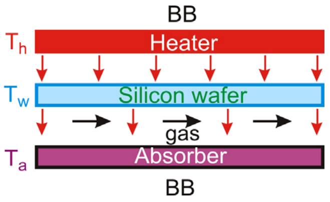

Fig. 1. Schematic representation of the lamp-heating reactor. The BB (blackbody) heater and absorber plates simulate the lamp block and the heat removal system, respectively. The input heat (vertical arrows) is defined by radiation emitted from the heater and transmitted through the wafer. The output heat is removed by radiation and, depending on the design of the reactor, by the cooling gas flow or heat conduction through the gas-filled gap between the wafer and absorber plate.

$$C_\nu \rho d \frac{dT}{dt} = P(T_W). \tag{1}$$

Here C_ν, ρ, d are the constant-volume specific heat of the wafer, the wafer density at the wafer temperature T_W, and the wafer diameter, respectively. The function of heat balance between the input and output heat fluxes, $P(T_W)$, is defined by the equation

$$P(T_W) = q_{in} - q_{out} - q_c, \tag{2}$$

where q_{in} and q_{out} are, correspondingly, the densities of radiation fluxes incident on the upper (input) surface of the wafer under study and emitted from its lower (output) surface and q_c is the density of the conductive/convective heat fluxes removed from the wafer.

In the case of supplementary conductive heat removal, we have [11]

$$q_c = (\alpha/b)(T_W - T_a), \tag{3}$$

where T_a is the absorber temperature and α and b are, correspondingly, the thermal conductivity of the gas in the gas-filled gap and the gap width.

In the case of supplementary convective heat removal, we have [11]

$$q_c = H(T_W - T_0), \tag{4}$$

where H is the heat exchange coefficient, i.e. the parameter describing the heat exchange between the wafer and the gas blowing it and T_0 is the gas temperature.

The above two heat fluxes can be placed into one-to-one correspondence, if it is assumed that, in the case of supplementary convective heat removal, (i) the absorber temperature T_a is equal to the temperature of the