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Subtle gate oxide defect elimination to improve the reliability of a 32M-bit SRAM product

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ABSTRACT

Tiny defects may escape from in-line defect scan and pass WAT (Wafer Acceptance Test), CP (Chip Probing), FT (Final Test) and SLT (System Level Test). Chips with such kind of defects will cause reliability problem and impact revenue significantly. It is important to catch the defects and derive the prevention strategy earlier in the technology development stage. In this paper, we investigate an SRAM with tiny defects which passed in-line defect scan, WAT, CP and FT but failed in HTOL (High Temperature Operation Life) test, one of the product reliability qualification items. FA (Failure Analysis) reveals gate oxide missing defect is the root cause. The goal is to pass reliability qualification and release product into production on schedule. The failure mechanism, optimization of gate oxide process, enhancement of defect scan and testing methodology will be introduced. Experiment results show very good HTOL performance by the combination of process and testing optimization.

1. Introduction

As the process technology node continue scaling down, the gate oxide thickness, critical width and space of devices become smaller, tiny defects play important roles as product yield killer and reliability failure stimuli. The chips with tiny defects cannot be screened out effectively either by wafer level or package level functional tests. That means some chips shipped to end users have a potential reliability issue over a certain period of time. This issue may affect the goodwill and finally lead to revenue decrease. It is important to look for the defect root causes and to derive the prevention strategy earlier in the technology development stage [1,2].

Since gate oxide is the core structure of MOS transistors and MOS transistors are the key devices for semiconductor IC products, gate oxide related defect is one of the most critical issues in the IC product manufacturing process. It is crucial to provide chips with good integrity and reliability of gate oxide for semiconductor manufacturers. Fig. 1 shows the dielectric breakdown strength distribution of MOS capacitor, in which the curves of group I and II present the devices with extrinsic defects. Since the extrinsic defects enhance electric field strength locally, the dielectric breakdown strength of defective MOS capacitors will become lower than that of normal ones. The breakdown voltage of defective chips in group I is very low so that they can easily screened out in CP and FT. However, defective chips in group II may pass general functional tests but fail at infant mortality stage and finally cause reliability problem. It is one of the important factors affecting the development and profitability of semiconductor manufacturing, since IC manufacturers will not have confidence to release products into production until they have passed reliability test. Gate oxide process optimization for these defects is rather time consuming, therefore, looking for an effective methodology through the combination of both process and testing optimization to catch the defective chips before shipping them to customers is crucial for a new product or process development [3–6].

A 32M-bit SRAM product which passed WAT, CP and FT but severely failed in HTOL 168 hours is used in this paper to validate the methodology, by which the reliability performance is improved to pass HTOL 2000 hours above. In the following sections, the failure mode and root cause of the reliability issue is firstly introduced. Then, the failure mechanism of the defect is given to derive the solutions from both process and testing point of view. Finally, the experiment results show that the tiny defects are successfully sieved out and the HTOL performance is improved significantly by means of this optimal methodology.

2. Tiny defects and root cause of defects

Some SRAM bits with tiny defects in the gate oxide may escape from both wafer sort test and final test, but they can be captured in

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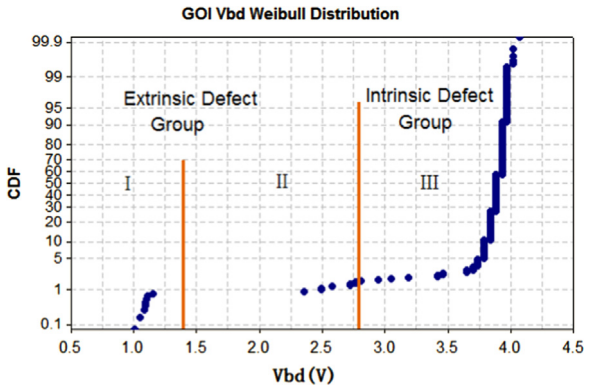

Fig. 1. Distribution of dielectric breakdown strength. The devices with extrinsic defects in group I will be screened out in CP or FT, defective chips in group II may pass general functional tests but cause reliability issue.

HTOL test. Besides, the defect density is quite low since there are only 1 or 2 transistors failed in the 32 M bit SRAM, traditional GOI (Gate Oxide Integrity) monitor cannot catch them during process qualification stage either. In order to identify the subtle defect precisely and quickly, many FA (Failure Analysis) skills are implemented and optimized for this issue [7–12]. As shown in Fig. 2, TEM and EELS (Electron Energy Loss Spectrometry) analysis results reveal that the gate oxide of defective transistor is missed. Since the defect is so tiny, in-line defect scan, WAT, GOI monitor, CP and FT may fail to catch it, which eventually causes product qualification failure.

3. Failure mechanism

According to FA results, the process conditions of gate oxide growth have to be optimized. Temperature, time and O2 pressure are known to dominate the interaction of O with Si surface. Fig. 3 illustrates that there are two distinct regions in pressure–temperature phase space, which indicates totally different O–Si interactions [13]. From thermodynamic perspectives, oxides such as SiO2 are stable in an oxygen rich environment under high temperature, where O interaction with wafer surface results in oxide growth.

$$Si(s) + O2(g) \rightarrow SiO2(s) \quad (1)$$

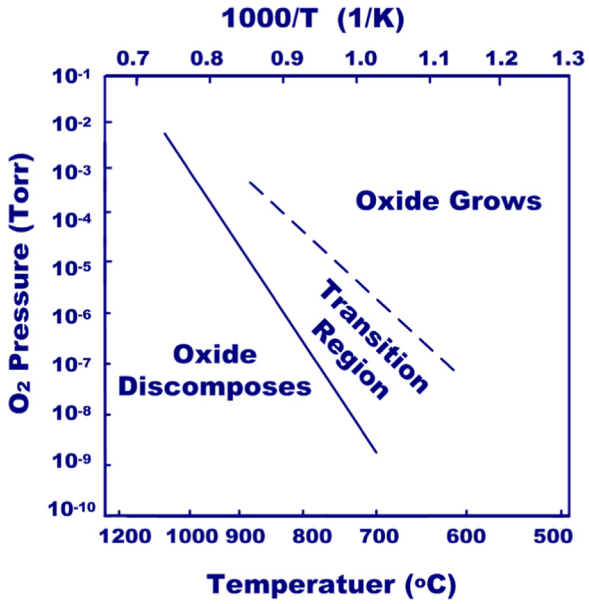

Fig. 3. Oxygen pressure–temperature phase diagram. SiO2 grows above the line and decomposes below the line.

If the reaction environment is deficient in oxygen, SiO2 will decompose into SiO. That is, surface etching via volatile SiO formation occurs and it causes gate oxide missing.

$$2Si(s) + O2(g) \rightarrow 2SiO(g) \quad (2)$$

4. Elimination and monitoring of gate oxide missing defect

4.1. Scheme A: Optimization from gate oxide process and defect scan methodology

Extra oxygen is introduced into ISSG (In-situ Steam Generation) oxide anneal process to eliminate the gate oxide missing defect, and then KLA-2835 defect scan is performed to check the experimental results. Fig. 4 shows that introducing the extra oxygen into ISSG oxide anneal step helps to eliminate the gate oxide missing defect. Because the device characteristics are required to

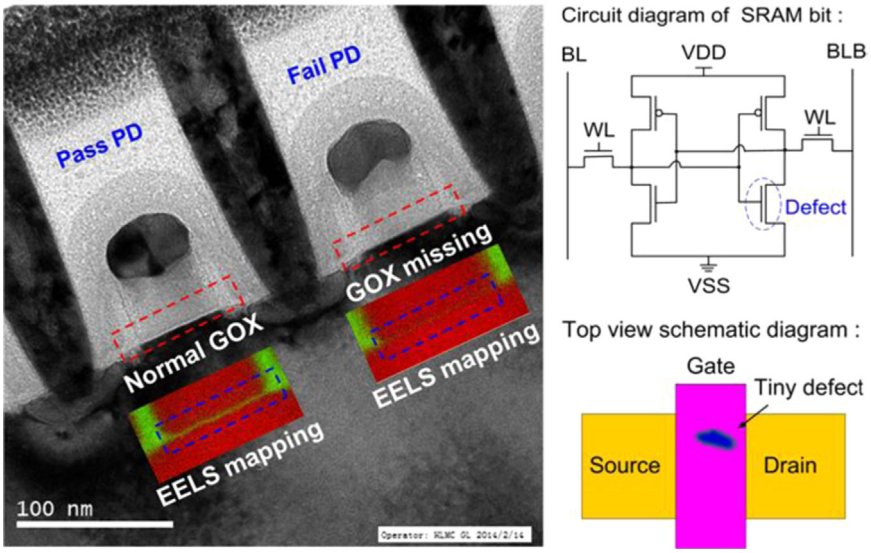

Fig. 2. The TEM and EELS (Electron Energy Loss Spectrometry) analysis results of the SRAM failure bit, tiny gate oxide missing defect is the root cause of HTOL test fail.