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Modeling of temperature profile, thermal runaway and hot spot in thin film solar cells

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ABSTRACT

Hot spot and thermal runaway are serious phenomena leading to the degradation of CdTe thin film solar cells. Here, we show that these issues are well related to temperature variation in the device structures mostly because of current flowing across transparent conducting oxide (TCO) layer or back contact of a CdTe device structure: glass/TCO/CdS/CdTe/graphene. Graphene nanolayer was chosen as the back contact because of its high thermal conductivity. We present a modeling of the temperature profile in CdTe thin film devices considering both uniform and nonuniform temperature distribution and current flowing across TCO layer. Temperature profile for hot spots at the edges of devices are modeled and compared to literature reports of both modelled and measured data. The model is based on the heat transfer equation (which uses thermal resistances) and in particular accounts for convection and conduction resistances by means of their ratio, the Biot number – a factor that could be optimized in the design of photovoltaic devices. Profiles were modelled taking into account both uniform and non-uniform temperature profiles for the glass, and currents flowing though the TCO. It is shown that the current flowing across the TCO layer can contribute to thermal runaway and its spreading to neighbouring areas. Overall the modelling data suggests that thin film solar devices could be designed to minimise hot spot runaway issues by taking into account the thickness and temperature dependence of the layers thermal conductivity, convection and conduction resistances. This can be extended to other solar cell structures or large scale modules.

1. Introduction

The hot spot runaway for thin film solar cells was first introduced and investigated both theoretically and experimentally by the research group of Prof. Karpov [1–3], thermal conduction in thin film solar cells was suggested to result in thermal runaway instability [4]. Any temperature fluctuation in the local areas of the film structure can increase the electrical conduction and cause shunting pathways or hot spots. These phenomena are known to degrade the device performance over time. Eventually, it is known that current robbing by hot spots makes them still hotter. The temperature variation in the structure is not a problem itself but it impacts also on the film morphology, stoichiometry and thermal resistance [7]. Normally, the temperature increase is reversible before physically impacting the atomic structure. The temperature profiling with IR camera is the common non-destructive method to detect the temperature distribution on the surface of the solar cells, particularly for hot spot detection [8,9]. Under real operation conditions, the irradiation and current flow through the diode will heat up the device because of Joule effect. The partial shading is another external problem that can cause nonuniform temperature distribution [10]. All those variations in the temperature can run away through the thickness and/or length of the solar cell and change the thermodynamic efficiency thus require to be modeled in order to obtain an insight into the physics of thermal runaway mechanisms. A solar cell under sunlight is heated up by absorbing the infrared wavelength or by the current flowing through the diode from the front contact to the back contact. The back contact was chosen to be a nanolayer of graphene which is conductive of heat so to reduce the hot spot creation probability. The heat is then transferred to the neighbor area by conduction or convection. Graphene is cheaper to deposit and has a high thermal conductivity and resistance. Graphene will reduce the ion migration from the conventional metallic back contacts i.e. Au or Cu and thus it avoids accumulation of the defects at the junction of CdS/CdTe. This reduces the degradation rate and a rather stable device under temperature and bias is obtained. A better coverage of the CdTe

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surface by graphene will reduce the induction of impurities on the surface and migration of defects into the CdTe bulk. Therefore a rather stable and reliable device is obtained [11].

Here, we propose a modeling approach to simulate the temperature distribution over the thickness of CdTe thin films. Such consideration is important because of the thin thickness of about 2 µm. The heat transfer from the glass substrate to the CdTe layer or from the joule heating (due to current flow from the TCO layer) can figure out the temperature profile of CdTe layer and influence on the performance, characteristics and reliability over time. We will study the uniform and nonuniform temperature profiles starting from the heat transfer problems. Then, the effect of hot spot created in the center or edge of the cell is considered and the Biot number is introduced representing the ability of thermal resistances in convection and conduction heat exchange. In this paper we propose applying graphene nanolayer as the back contact. This nanolayer is a great heat conductive and reduces the hot spot creation probability.

2. Modeling the thermal profile

The distribution of the temperature, T, in a solid is a function of the position, r, and time, t defined by the heat diffusion equation [3]:

$$-k\nabla^2 T(t,r) + Q(r) = \frac{d}{dt}c_p T(t,r) \tag{1}$$

where k is the thermal conductivity of the material as a function of temperature [W/(m K)], c_p is the specific heat [J/(kg K)] and Q is the heat generation rate. Both k and Q are position dependent (e.g. as a function of r). Then, we may extend Eq. (1) in three-dimensional space of (x,y,z) in the steady state condition ($\frac{dT}{dt}=0$) as [3]:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + Q^* = 0 \tag{2}$$

where Q^* is the rate of heat generation per unit volume (W/m^3). This equation is subject to specific initial values and proper boundary conditions. For CdTe and CdS semiconductors, k is an exponential function of temperature and position [14]. However, in our study the temperature variation range is rather small which allows us to assume k to be a constant through the device. This is because the temperature variation through the device is mostly from the glass substrate which is under the irradiation of the sunlight. In addition, the thin film device has a thin thickness which practically can exchange heat with the environment 'only' through the bottom and upper faces (i.e., the glass substrate and back side). Therefore, we get $k=16$ W/m K equal for CdTe and CdS layers. The one-dimensional heat diffusion equation is given as:

$$\frac{d^2T}{dx^2} = -\frac{Q^*}{k} \tag{3}$$

To derive Q^*, consider Fig. 1 showing the structure of the thin film device with a glass/TCO/CdS/CdTe/Metal. The CdTe thin film is deposited on the glass/TCO substrate through CdS window layer as n-type. Q^* includes Joule heating due to power dissipation in the TCO layer. This is due to the fact that the photo-current collected from the solar cell has to flow through the TCO layer, with the lateral resistance R_1, and to be collected by the external wires. Moreover, the glass substrate which is under illumination is heated up and transfers this heat to the upper layers such as CdS and CdTe. We assume that TCO is thermal conductive as it is also electrical conductive. Thus, the power loss is arisen when thermal exchange between the glass and the CdTe layer through CdS thickness, t_2. The power dissipation, P_{diss}, in a partial TCO length, Δx, can be expressed as:

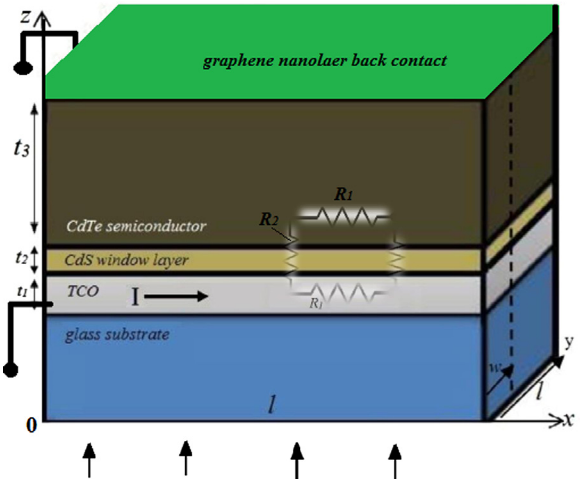

Fig. 1. Schematic of the CdTe thin film structure. The heat transfer is considered in the x-direction for a volume of $(w.\ \Delta x.\ l)$.

$$P_{diss}(x) = I^2\Delta R_1(x), \quad \text{where } \Delta R_1(x) = \rho_0\frac{\Delta x}{w.\ t_1}. \tag{4}$$

where I is the collected photo-current from the semiconductor CdTe layer which is flowing under bias and is now passing through the TCO electrode. Note that the photo-current generated in the semiconductor is collected by the lateral electrodes, one of which is resistive TCO. t_1 is the thickness of TCO, w is the width, ρ_0 is the electrical resistivity of TCO layer at reference temperature, $\rho \sim 10$ $\Omega/\square$.

On the other hand, energy loss, P_{loss}, due to the heat transfer between the glass substrate and the CdTe layer through CdS n-type layer for a partial length, Δx is given by,

$$P_{loss}(x) = \frac{T(x) - T_{sub}}{\Delta R_2(x)}, \quad \text{where } \Delta R_2(x) = \frac{t_2}{k'.\ \Delta x.\ w} \tag{5}$$

where t_2 is the thickness of CdS window layer, k' is the thermal conductivity of CdS layer which has similar values to the thermal conductivity of CdTe for a wide range of temperatures as was studied by a few researchers in Refs. [15,16]. Based on the above equations, the net heat energy gain per unit volume can be obtained. The unit volume was taken as the volume of CdS layer. The reason is that, practically, at the junction of the window and absorber layers, the temperature profile of CdTe surface will be the same as the upper face of the CdS layer. As the geometry and properties of the device are similar in x and y directions, the heat transfer will be considered only in a thin longitudinal volume of $w.\ \Delta x.\ t_2$. The same analysis can be done in the y direction with $w.\ \Delta y.\ t_2$ but with the same results. Hence, the heat generation rate per unit volume, for a partial length of the layer underlying CdTe film, will be,

$$Q^*_{eff} = \frac{P_{diss} - P_{loss}}{w.\ \Delta x.\ t_2}. \tag{6}$$

The temperature distribution, $T(x)$, on the surface of CdTe layer immediately over CdS layer can be obtained using the simplified heat equation (3). The summarized heat flow equation is as follows:

$$\frac{d^2T(x)}{dx^2} = \lambda^2 T(x) - \lambda^2 T_{sub}(x) - \theta \tag{7}$$