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Short communication

Amorphous InGaZnO thin film transistors with sputtered silver source/drain and gate electrodes

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ABSTRACT

The amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) with sputtered silver source/drain (S/D) and gate electrodes were investigated and developed. The sputtered single-film Ag was confirmed to be unfit for the electrodes of a-IGZO TFTs because of its bad contact with a-IGZO and atom diffusion into insulators. Accordingly the sputtered Mo films were proposed to serve as the capping layers, indicating that the 20-nm-thick Mo could effectively form ohmic contact with the a-IGZO, prevent the Ag diffusion into the SiO_x, and make good adhesion to the glass substrates. The devices with multi-layer S/D and gate electrodes (Mo/Ag/Mo) were successfully fabricated, exhibiting the reasonably good performance and thus proving the application of the sputtered silver electrodes into a-IGZO TFTs was possible.

1. Introduction

Amorphous InGaZnO (a-IGZO) is expected to be used as the active layers of thin film transistors (TFTs) addressing active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diodes (AMOLEDs) [1,2]. To drive large-sized flat panel displays (FPDs), the development of highly conductive electrodes for a-IGZO TFTs seems quite necessary [3,4]. Therefore, the a-IGZO TFTs with copper source/drain (S/D) and gate electrodes have been widely investigated and developed [5–7]. On the other hand, silver, with even better conductivity than copper, should also be considered. The smallest resistivity of the silver electrodes could lead to the lowest resistance-capacitance (RC) delay in the TFT array, which is one of the most serious issues to be solved for large-size and high-resolution FPDs. In addition, it has been found that the silver films are easy to be deposited and patterned by wet etching [8–10]. Therefore, development of the silver electrodes for a-IGZO TFTs are quite meaningful and possible. Recently, some related studies have been reported, but unfortunately none of their silver depositions adopted sputtering, the most likely preparation technique for industrial productions [8–10]. It is worth noting that our group proved that the wet-etched silver electrodes could be used for a-IGZO TFTs, where the Ag films were deposited by an E-beam evaporator [8]. In this study, we tried to develop the sputtered silver electrodes used for a-IGZO TFTs, whereas we found that the single-film Ag electrodes prepared by sputtering could lead to some severe problems including the bad contact with a-IGZO and the atom diffusion into insulators. Accordingly, the sputtered Mo/Ag/Mo S/D and gate electrodes were proposed to solve these problems, with which the reasonably well-performed a-IGZO TFTs were successfully fabricated.

2. Experimental

There were two types of inverted-staggered a-IGZO TFTs prepared in this study. The devices of Type I were fabricated on the heavily doped (n++) silicon wafers (gate electrodes) with 300-nm-thick thermal SiO_2 films (gate insulators), as shown in Fig. 1(a). Being the active layers, the 50-nm-thick a-IGZO films were deposited with RF power of 60 W by a magnetron sputtering system using a target of In: Ga:Zn=1:1:1 in atomic ratio. The 100-nm-thick S/D electrodes were deposited by another DC sputtering system. The films for the devices of Type I were patterned by the shadow masks, leading to the channel width/length of 275 μm/1000 μm. The TFT devices of Type II were prepared on glass substrates (Corning eagle 2000), as shown in Fig. 1(b). First, the gate electrodes were prepared in the DC sputtering chamber. Then the 400-nm-thick SiO_x films were prepared as the gate insulators by RF sputtering at 250 °C, followed by the deposition of 60-nm-thick a-IGZO films (active layers) by RF sputtering at 150 °C. Next, the S/D electrodes were prepared in the DC sputtering chamber. Finally the 120-nm-thick SiO_x films were deposited as the passivation layers by RF sputtering. The standard photolithography [11] and wet etching were used to pattern the films for the a-IGZO TFTs of

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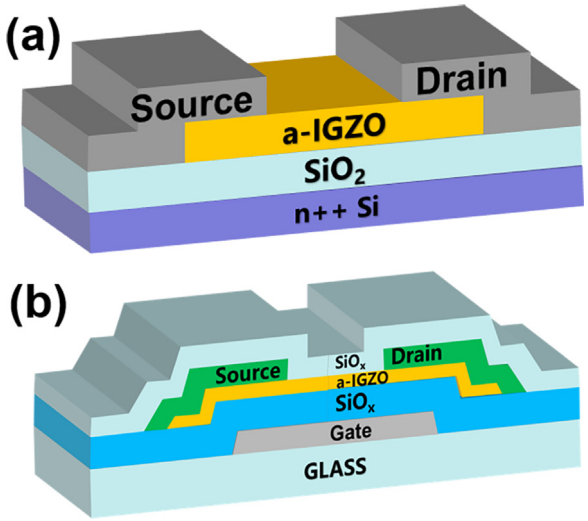

Fig. 1. Schematic cross sections of the a-IGZO TFTs, patterned by (a) shadow masks (Type I) and (b) photolithography/wet etching (Type II).

Type II, resulting in the channel width/length of 10 μm/400 μm. All the samples were annealed in air at 400 °C for 1 h to improve the device performance.

The TFT electrical characteristics were measured by a Keithley 4200 analyzer at room temperature (RT), from which the performance parameters, such as field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold slope (SS), and on-off current ratio (I_{on}/I_{off}) were extracted as Ref. [12]. The interfacial structure between the S/D electrodes and the a-IGZO was observed by a ZEISS Auriga SEM/FIB crossbeam system.

3. Results and discussion

First, we investigated the a-IGZO TFTs with silver S/D electrodes using the devices of Type I. As shown in Fig. 2, the a-IGZO TFTs with single-film Ag S/D electrodes exhibited very poor electrical behavior, i.e. a poor μ_{FE} of 0.5 $cm^2/V \cdot s$ and a too large V_{th} of 22.8 V. Such inferior performances could be assumed to result from the bad contact at the a-IGZO/Ag interface. The cross-sectional scanning electron microscopy (SEM) images in Fig. 3 clearly demonstrated the Ag film became very irregular after annealing in

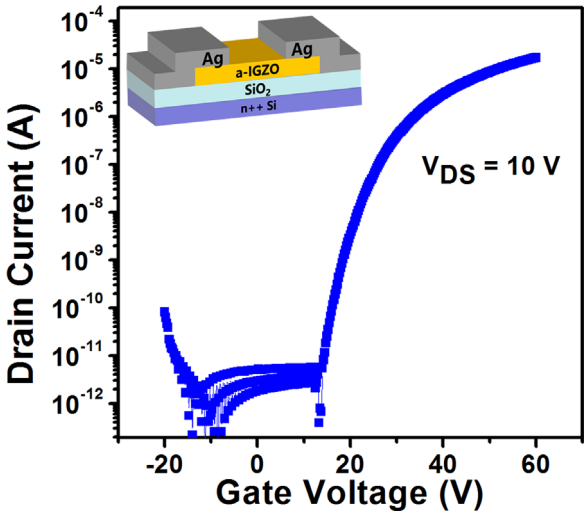

Fig. 2. Transfer curve of the a-IGZO TFTs with the single-film Ag S/D electrodes (inset: the schematic cross section of the devices).

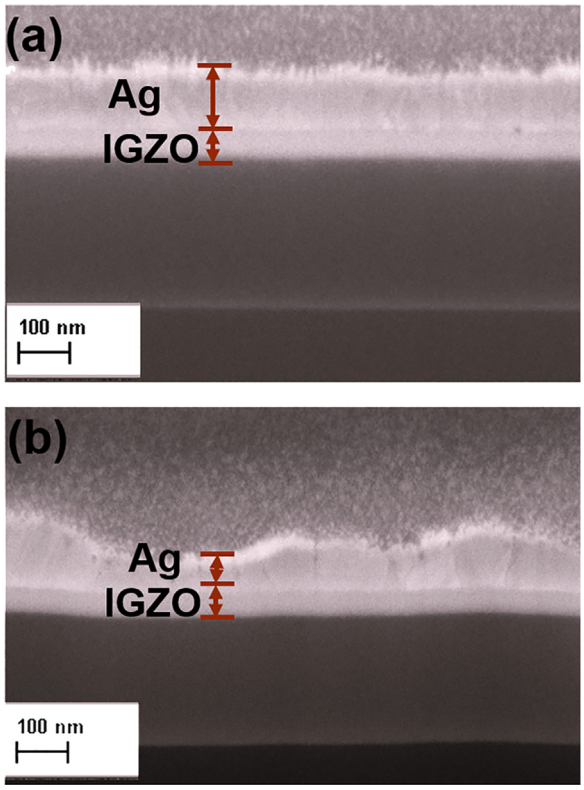

Fig. 3. Cross-sectional SEM images of the interface between the Ag and the a-IGZO films for (a) the as-deposited sample and (b) the one being annealed in N_2 at 400 °C for 1 h.

N_2 at 400 °C for 1 h, which tended to cause the bad contact with the a-IGZO layer. Since the annealing process is necessary for the TFT fabrication, it was quite reasonable to assume that the inferior performance of the a-IGZO TFTs with the single-film Ag S/D electrodes was mainly due to the bad contact between Ag and a-IGZO. In addition, a possibly formed thin insulating layer like AgO_x (10^{-2}–10^{8} Ω•cm) [13] at the a-IGZO/Ag interface might also result in the large contact resistance. Thus, it was proved that the direct contact between the Ag film and the a-IGZO layer should be avoided to choose the materials for the S/D electrodes of a-IGZO TFTs.

The effect of the contact material on the performance of a-IGZO TFTs was demonstrated in Ref. 13, where the devices with Ag, Ti, and Mo S/D electrodes were investigated. The source and drain resistances ($2R_{s/d}$) of the Ag, Ti, and Mo samples reached 4×10^4, 2×10^4, and 1×10^4 Ω, respectively [13]. This implied that a spatial potential barrier existed at the interface of a-IGZO/Ag, which, however, could be evidently lowered if Ti (or Mo) S/D electrodes were adopted. In this study, we tried to use Ti (or Mo) as the interlayer between a-IGZO and Ag, aiming to improve the contact properties between the silver S/D electrodes and the active layers. The a-IGZO TFTs (Type I) with variously thick Ti (or Mo) interlayers were prepared here. Fig. 4 shows the I_{DS}-V_{GS} curves of the a-IGZO TFTs (Type I) with single-film Ag, single-film Ti (or Mo), and Ag/Ti (or Ag/Mo) bilayer electrodes. The corresponding performance parameters were extracted and listed in Table 1. By depositing a Ti interlayer, the electrical characteristics of the a-IGZO TFTs became much better, i.e. larger I_{on} and smaller V_{th}. One might assume here that the contact resistance between the metal electrodes and the a-IGZO was effectively reduced by the formation of a TiO_x interfacial layer, which led to an oxygen deficient region in the a-IGZO contact area [10]. On the other hand, the a-IGZO TFTs with the Mo interlayers showed the similar but even better tendency, as shown