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Electrochemical mechanism of layout-dependent corrosion of tungsten in contact plugs

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ABSTRACT

The investigation elucidates electrochemical effect on tungsten (W) contact plugs and proposes front-end-of-the-line semiconductor manufacture processes that are responsible for corrosion involving source/drain implants, rapid thermal anneal (RTA) and nickel silicide (Ni_xSi_x). W-filled contacts are commonly used in submicron and even nanometer CMOS technology, and the integrity of W contact plugs becomes increasingly critical as transistors continue to shrink. Incomplete W plugs with a recess on the tops of the contacts were observed in N+/n-well locations following W chemical mechanical polishing (WCMP). This phenomenon arises from anodic corrosion since the under-layer P+/p-well and N+/n-well form a PN junction structure, which has built-in potential and promotes the movement of photo-generated electrons during WCMP. The mechanism of the electrochemical effect is elucidated, and a series of experiments indicates a thin Ni_xSi_x layer, a heavy dosage of source/drain implants and a high RTA temperature promote the formation of corrosion defects.

1. Introduction

Tungsten (W) has for a long time been used as a metallization material in the semiconductor process. With a high melting point of 3385 °C and a low resistivity of 5.5 μΩ/cm, W is resistant to electromigration and resistive–capacitive delay. The superior step-coverage capability of chemical vapor deposited (CVD) W [1] satisfies the requirements of contacts with high aspect ratios as the scale of semiconductor technologies is reduced. The submicron CMOS process therefore uses W to fabricate contacts and via plugs as conductive connections between the first metal and the substrate or different metal layers. Even as the technology node entered nanometer scale with a back-end-of-the-line via and line interconnections of copper (Cu), W remains used to fabricate contact plugs. One potential concern is that the resistance of W contacts with high aspect ratios (AR) increases as the technology node approaches and goes beyond 32 nm [2]; nevertheless, W is still used more often than its alternatives. The integrity of W contact plugs is therefore very important especially as MOS transistors become smaller.

The corrosion of W has been one of the most widely studied issues related to W chemical mechanical polishing (WCMP) since it was developed to replace the etch-back part of the submicron CMOS process [3]. In WCMP, both galvanic and intrinsic corrosions occur; these are caused by the difference between the electrochemical potentials of W and the contact barrier layer metal of titanium nitride (TiN) [4], the content amount of deposited W [5], and the electrochemical properties of slurries in concentrated H_2O_2 solution [2]. Even after WCMP, the queue time that wafer exposed in the ambient illumination [6], the metal etching process and the cleaning solvent can lead to corrosion of W plugs [7–9]. Various investigations have shown that electrochemical corrosion may be caused

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by W metal deposition, WCMP and many subsequent steps.

This study proposes that the FEOL processes of the semiconductor device fabrication prior to the deposition of W also contribute to W corrosion. The mechanism of layout-dependent corrosion is elucidated, and FEOL process experiments regarding Ni_xSi_x thickness, implantation dosage, and RTA temperature were conducted and discussed.

2. Experiment

A total of 300 mm patterned wafers were processed until the step of contact WCMP thorough a shrinkage 55 nm CMOS process flow in the experiment. The process modules for the fabrication of contact plugs involve conventional processes of patterning holes by immersion lithography, inter-layer-dielectric (ILD) etching, barrier titanium/titanium nitride (Ti/TiN_x) metal, W deposition, and WCMP. The wafers were then scanned by the inline defect inspection after WCMP.

A bright-field (BF) defect inspection tool with a 120 nm fine pixel was utilized to quantify the count and distribution of W corrosion defects. An inline scanning electron microscope (SEM) was then used to capture a top-view image of the defect features, and an offline transmission electron microscope (TEM) with high resolution was used to examine the cross-sections of W plugs. The wafer acceptance test (WAT) tool, an Agilent HP4082A, was used to measure the contact resistance. The metrology tool basic on ellipsometry optics, an Aleris 8500, was used to measure the oxide thickness on silicon wafers.

3. Result and discussion

3.1. Layout-dependent corrosion of contacts

Corrosion defects were found using the inline inspection tool following WCMP only at the same place in the chips. Fig. 1 presents corrosion defects with layout dependency in the static random access memory (SRAM) area, and the cross-section reveals a 180 Å recess on top of the W plug. Those contacts in SRAM can be categorized as cell and pickup contacts, as shown in Fig. 1(b), in which cell contacts are above the N+/p-well or the P+/n-well by either N or PMOS, respectively; while pickup contacts are above either the N+/n-well or the P+/p-well. Restated, cell contacts connect to the source/drain that with the different type of well implantation, but pickup contacts connect to the source/drain that with the same type of well implantation. This point decides the energy barrier in the substrate and related to the resistance to electrochemical effect.

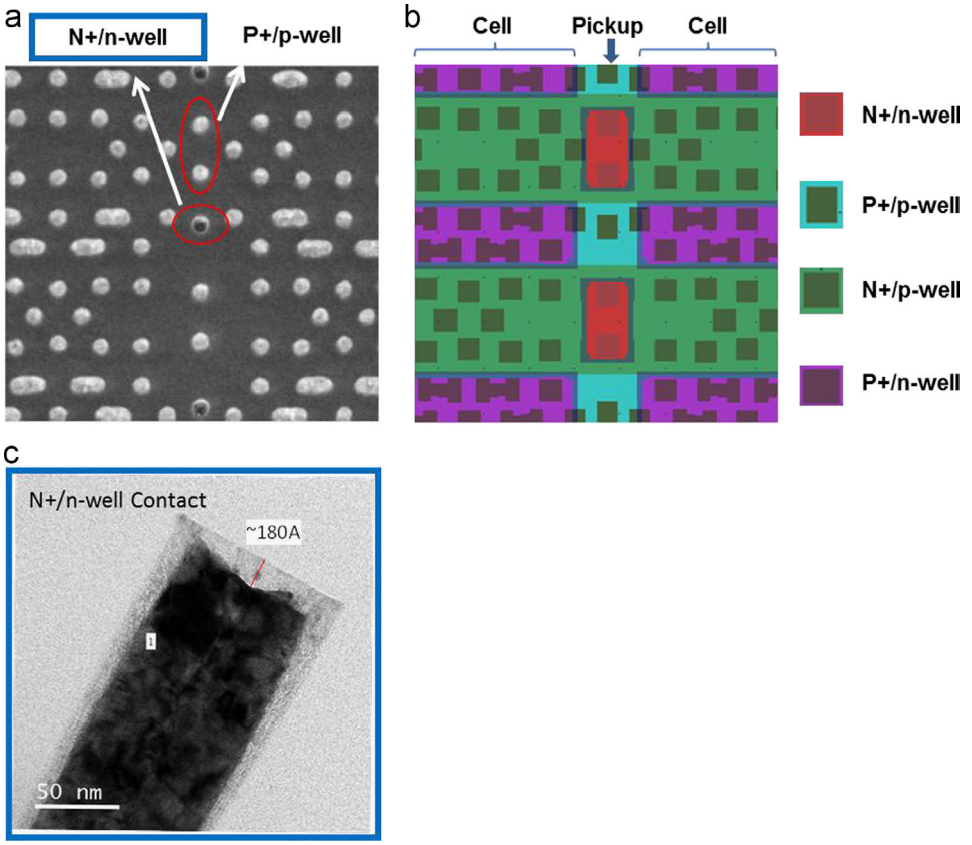

Fig. 1. W corrosion on the N+/n-well pickup contact plugs (a) top-view SEM image at WCMP, (b) the corresponding GDS layout of multi-mask layers, and (c) TEM cross-section image.