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Review

A novel 4H-SiC MESFET with a L-gate and a partial p-type spacer

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ABSTRACT

A 4H-SiC MESFET incorporated with L-gate and partial p-type spacer (LP-MESFET) is proposed and simulated. The simulations show that obvious improvements can be obtained for the LP-MESFET compared to the conventional structure (C-MESFET), such as a 17% larger of the saturation current, a 36% higher of the breakdown voltage V_b and a 95% larger of the maximum output power densities. Furthermore, the decrease of the gate-drain capacitance (C_{GD}) will lead to an improved RF performance for the LP-MESFET.

Contents

1. Introduction

Owing to the superior characteristics of SiC, such as wide band gap (3.26 eV),large thermal conductivity (3.5 W/cm K), high breakdown electric field (3 MV/cm) and high electron saturation velocity (2.1×10^7cm/s), SiC based MESFET offers a promising solution to the need for compact high power density RF devices [1–3]. To obtain higher output power density, 4H-SiC MESFETs must be able to sustain large drain current and have high breakdown voltages. High drain current requires a large product of the channel doping and thickness ($N \times a$). However, a higher channel doping concentration will reduce V_b, and a thick channel layer will lead to a lower aspect ratio of gate length to channel thickness (L_g/a) and result in short-channel and drain-induced barrier lowering (DIBL) effects, which will degrade the device and circuit's performance [4]. In recent years, many structures have been reported, such as buried-gate structure [5,6], double recessed structure [7] and so on. However, when the structures are used, some performances of SiC MESFETs can be improved obviously, but some sacrificed at the same time. For examples,the buried-gate structure can suppress the surface trapping, and the double recessed structure can increase the drain saturation current, but they all lead to lower breakdown voltages [8]. So, how to improve SiC MESFETs' performances comprehensively is still a challenge to the device designer.

In this paper, a 4H-SiC MESFET combined with L-gate and partial p-type spacer (LP-MESFET) is firstly proposed. The L-gate can reduce the depletion layer under the gate and decrease the gate capacitance. Because of a wider conduct channel released under the L-gate, the saturation

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drain current can be increased effectively. The L-gate structure has lower and upper gates, which effectively controls a thinner and a thicker part of the channel, respectively [9]. Since a p–n junction can be formed between the p-spacer and the n-channel, a distinct reduction of the gate-drain capacitance will be achieved. Therefore, both of the L-gate and p-spacer are especially propitious to the improvement of the DC and RF performances of SiC MESFETs.

2. Device structure

Schematic cross-sections of conventional and proposed 4H-SiC MESFET structures are shown in Fig. 1. These structures consist of a high-purity semi-insulating substrate, a 0.5 μm p-buffer with a concentration of $1\times10^{15}\ cm^{-3}$, a n-channel with a thickness of 0.2 μm and a doping level of $2.4\times10^{17}\ cm^{-3}$, the doping level of N^+ contact layer is about $10^{19}\ cm^{-3}$. All the devices have a gate-to-source spacing (L_{GS}) of 0.5 μm and gate-to-drain spacing (L_{GD}) of 1.5 μm, respectively. The dimensions of the two L-gates are the same as follows: length of the upper gate is 1.0 μm and that of the lower gate is 0.5 μm, the height of the step is 0.1 μm. For the LP-MESFET the partial p-type spacer has a doping level of $2.4\times10^{17}\ cm^{-3}$ and a thickness of 0.1 μm, and it has a 0.8 μm length and is 0.4 μm far from the gate. A 2D simulator ISE (Integrated Systems Engineering) TCAD Release 10.0 is used to simulate the devices, a temperature of 300 K was employed by default in simulations. In addition to the basic Possion and the carrier continuity equations, several parameter models are used, such as Doping Dependence and High Field Saturation for mobility, In complete for incomplete ionization, SRH (Shockley-Read -Hall), Auger, gate electric barrier tunneling and barrier lowering for generation and recombination, and Avalance for impact ionization.

3. Results and discussion

Fig. 2 shows the simulated I_D–V_{DS} characteristics of C-MESFET, L-gate-MESFET and LP-MESFET under the gate bias (V_{GS}) vary from 0 to −12 V with a step of 4 V. It can be seen that due to the increased thickness of the gate-drain drift region and a wider channel opening outside the L-gate region, the LP-MESFET has 17% higher saturation drain current (I_{Dsat}) than that of conventional counterpart at $V_{GS}=0$ V. It also should be noted that, owing to a p–n junction formed between the p-spacer and n-channel, the saturated drain current of the LP-MESFET is slightly decreased comparing with that of the L-gate-MESFET, which leads to a reduction in effective thickness of the gate-drain drift region. Therefore, the LP-MESFET provides larger $I_{Dsat.}$ than the C-MESFET while maintaining comparable threshold voltage (V_T).

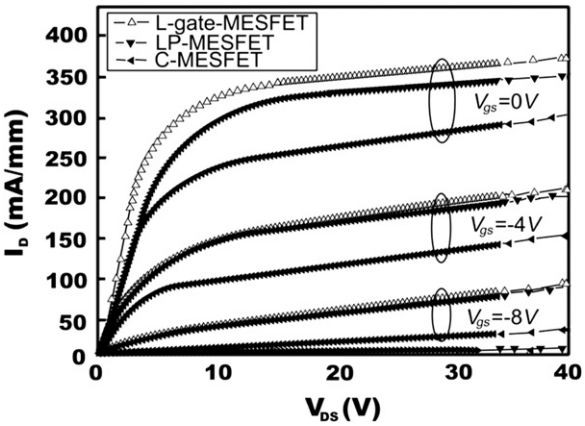

Fig. 2. The simulated I_D–V_{DS} characteristics of different structures.

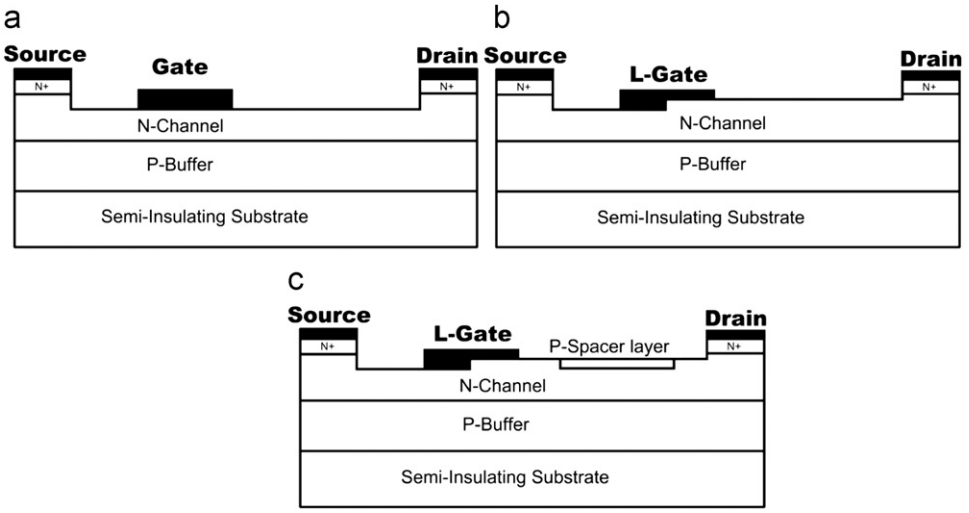

Fig. 1. Cross-sectional view of (a) conventional 4H-SiC MESFET (C-MESFET), (b) L-Gate 4H-SiC MESFET, (c) 4H-SiC MESFET with L-gate and partial p-type spacer (LP-MESFET).