Materials Science in Semiconductor Processing 15 (2012) 27–31

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Effects of the post nitridation anneal temperature on performances of the nano MOSFET with ultra-thin (<2.5 nm) plasma nitrided gate dielectric

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ARTICLE INFO

Available online 25 June 2011

Keywords:
Gate leakage
PNA
DPN
Ultra-thin gate oxide

ABSTRACT

A post nitridation annealing (PNA) is used to improve performances of the metal oxide semiconductor field effect transistor (MOSFETs) with nano scale channel and pulsed radio frequency decoupled plasma nitrided ultra-thin (<50 Å) gate dielectric. Effects of the PNA temperature on the gate leakage and the device performances are investigated in details. For a n-type MOSFET, as the PNA temperature rises from 1000 to 1050 °C, the saturation current and gate leakage are increased and reduced 7.9% and 3.81%, respectively. For a p-type MOSFET, the improvement is more significant i.e., 16.7% and 4.31% in saturation current increase and gate leakage reduction, respectively. The significant improvements in performance are attributed to the higher PNA temperature caused Si/SiON interface improvement and increase of EOT. Most of all, the high temperature PNA does not degrade the gate oxide integrity.

1. Introduction

In the past, scaling down the device's dimension is an effective way to increase the complementary metal oxide semiconductor (CMOS) device density, and enhances the driving capability. However, as moving down to the nano meter scale, the thickness of gate oxide is reduced to less than 14 Å for a 90 nm gate length device, which generates a large amount of gate tunneling current to weaken the integrity of gate dielectric and degrading the device's performance [1,2].

Hence, use of a high k (high dielectric constant) material to provide a physically thicker film for the same electrically equivalent SiO_2 thickness for reduction of leakage current becomes necessary and has been studied widely [3,4]. However, acceptable device mobility and reliability for the high k devices are still not meeting the production requirement [5].

Therefore, before the high k metal gate becomes a mature technology, silicon oxynitride incorporated with high nitrogen concentration (termed as SiON) and relatively high dielectric constant is still an attractive near-term candidate. Recently, decoupled plasma nitridation (DPN) [5] and remote plasma nitridation (RPN) [6] have been considered more to prepare SiON layer. Specifically the DPN demonstrates better across-wafer nitrogen uniformity and is more scalable than RPN approach.

In general, DPN is implemented using inductive coupling plasma to generate ions with lower kinetic energy for minimizing the carrier mobility degradation. However, the process is also a low temperature technology, which will induce defects in the SiON, and thus requiring a post nitridation anneal (PNA) at ~1000 °C to remove them [7]. However, we find if a higher temperature PNA is applied, the device saturation current and gate leakage could be improved more significantly.

In this paper, we investigate the effects of the PNA temperature and its related mechanisms on gate leakage, driving current, gate to junction overlap capacitance, gate

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doi:10.1016/j.mssp.2011.06.001

oxide integrity, and junction leakage current of a short channel MOSFET in details.

2. Experiments

As schematically illustrated in Fig. 1, the samples of nano MOSFETs with ultra-thin SiON gate dielectrics were prepared by a foundry's 65 nano CMOS technology. To form the ultra-thin SiON gate by a DPN process; firstly, a thin silicon oxide film with thickness less than 2.5 nm (see Fig. 2) was grown in low pressure N_2O ambient at a temperature of 1000 °C by rapid thermal process on (1 1 0)-oriented p-type, 8–12 Ω-cm 300 mm wafer. Next, the thin oxide film was nitrided with a mixture of N_2 and He plasma to form SiON. The plasma was excited by a microwave with 550 W RF power. Then, the samples were submitted to PNA process in a low pressure mixture gas (N_2/O_2=15,000–20,000 sccm/50–200 sccm) ambient under various temperatures (1000–1050 °C). The effects of different PNA temperatures on the ultra-thin SiON were investigated. We use SIMS (secondary ion micro-electric spectrum) to analyze nitrogen concentration depth profile in the SiON. Sequentially, a layer of 1000 Å n+poly silicon was deposited on the top of the SiON to finish the n+poly/SiON stack gate. In final, we used a foundry's 65 nano CMOS process to complete the MOSFET devices with a dimension of W/L=1 μm/0.07 μm.

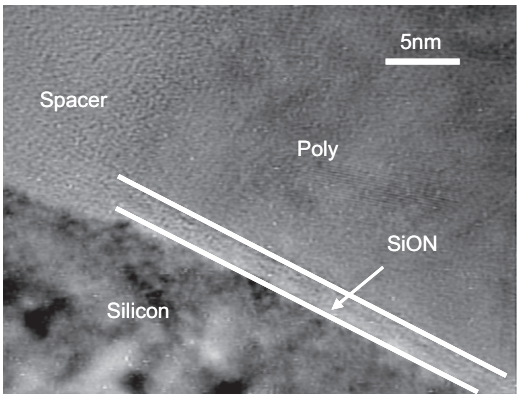

Fig. 2. TEM photo to show the dimension of the poly Si/SiON stack gate structure.

The devices electric performances are characterized by an HP4156 semiconductor parameter analyzer. The off leakage (I_{off}) was measured under voltage condition of V_d=1 V, V_g=V_s=V_b=0 V, with the gate leakage (I_{gi}) under V_g=1.2 V, V_d=V_b=0 V, and V_s=floating, where, V_s, V_g, V_d, and V_b are source, gate, drain, and substrate bias, respectively.

In addition, to investigate the temperature on the adverse effects of the PNA, we measured and compared the overlap capacitance of polygate to junction (C_{gdo}) and the gate breakdown field for various PNA temperatures. For measurement of the C_{gdo}, the gate and substrate biases are set at V_{DD} and 0 V, respectively. Then apply a small signal at drain side and measure the capacitance between gate and drain. While for examination of the gate oxide integrity, set V_b=V_s=V_d=0 V, and swept V_g to get the gate breakdown voltage under I_g=0.1 μA.

3. Results and discussions

Fig. 3 shows the SIMS depth profile of the elements (Si, O, and N) contained in the ultra-thin SiON layer as a function of PNA temperature. Clearly, as the temperature rose from 1000 to 1050 °C, the *N* element decreases firstly, and then increase slightly within a depth of ~20 Å above the SiON/Si interface. Besides, as indicated in Fig. 4, the equivalent oxide thickness (EOT) of the SiON layer measured by C–V method increases 0.6 and 0.8 Å for p and nMOSFET, respectively. This means, the higher temperature PNA forms a new thin oxide layer (0.6–0.8 Å) to increase the EOT, and also changes the N atoms profile in the SiON layer, i.e., the *N* atoms is pushed further away from the Si/SiON interface.

Figs. 5 and 6 indicate the gate leakage (I_{gi}) and the device saturation current (I_{dsat}) are reduced and enhanced with the PNA temperature for both p- and n-MOS samples, respectively. For example, as the PNA temperature risen from 1000 to 1050 °C, for n/pMOSFETs, the I_{gi} and I_{dsat} are reduced and enhanced up to 3.81%/4.31% and

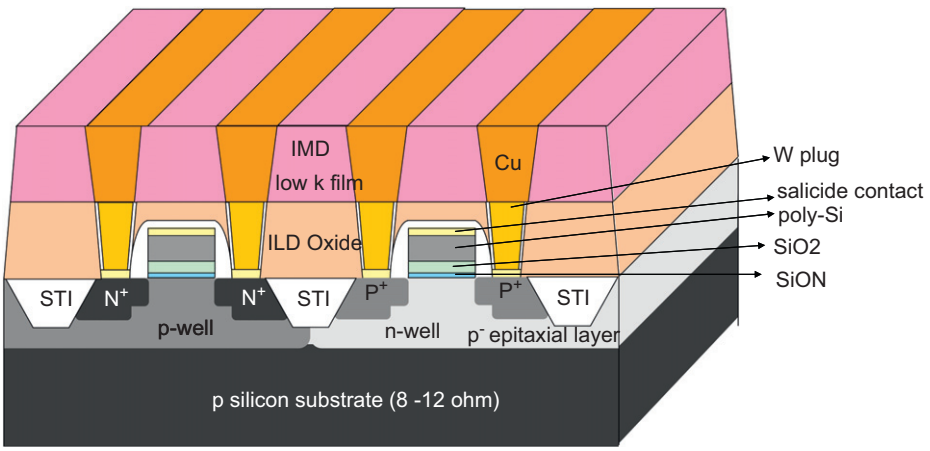

Fig. 1. Scheme diagram of the nano MOSFETs with ultra-thin SiON gate dielectrics prepared by a foundry's 65 nano CMOS technology.