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Frequency and voltage dependence of negative capacitance in Au/SiO_2/n-GaAs structures

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ABSTRACT

The frequency (f) and bias voltage (V) dependence of electrical and dielectric properties of Au/SiO_2/n-GaAs structures have been investigated in the frequency range of 10 kHz–3 MHz at room temperature by considering the presence of series resistance (R_s). The values of R_s, dielectric constant (ε'), dielectric loss (ε'') and dielectric loss tangent ($\tan\delta$) of these structures were obtained from capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements and these parameters were found to be strong functions of frequency and bias voltage. In the forward bias region, C–V plots show a negative capacitance (NC) behavior, hence ε'–V *plots* for each frequency value take negative values as well. Such negative values of C correspond to the maximum of the conductance (G/ω). The crosssection of the C–V plots appears as an abnormality when compared to the conventional behavior of ideal Schottky barrier diode (SBD), metal–insulator–semiconductor (MIS) and metal–oxide–semiconductor (MOS) structures. Such behavior of C and ε' has been explained with the minority-carrier injection and relaxation theory. Experimental results show that the dielectric properties of these structures are quite sensitive to frequency and applied bias voltage especially at low frequencies because of continuous density distribution of interface states and their relaxation time.

1. Introduction

Metal–semiconductor (MS) structures have great importance both in the modern electronic applications and in understanding solid-state electronic devices. When a native or deposited interfacial insulator layer, such as SiO_2, SnO_2 and Si_3N_4, is inserted between metal and semiconductor, the MS structures turn into a metal–insulator–semiconductor (MIS) or metal–oxide–semiconductor (MOS) structure depending on the thickness of the interfacial insulator layer. Existence of such insulator layer also causes capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of these structures to deviate considerably from the ideal behavior of MS structures. This deviation mainly takes the form of an uncommonly large intercept voltage, and nonlinearity C^{-2}–V plots in the inversion region [1–4]. Barrier height (Φ_B), thickness of interfacial insulator layer (d_{ox}) and series resistance (R_s) of structure are important parameters such that they cause both electrical and dielectric properties of these structures to be non-ideal. Admittance measurements provide a powerful spectroscopic method for the nondestructive testing of semiconductor devices and evaluation of their structural, electrical and dielectric parameters.

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Since MIS and MOS structures consist of a semiconductor between rectifier and ohmic contacts, interface states and bulk traps are formed in the structure, and these interface states and bulk traps, where charges can be stored and released when the appropriate forward bias and the external ac oscillation voltages are applied, have a large effect on devices [2,5–9]. More recently, some researchers have reported a negative capacitance (NC) behavior in the forward bias C–V plots of MS diodes [5,10–13], hetero-junctions [14,15], far-infrared detectors [16,17], laser diodes [18,19], light emitting diodes [20,21] and photo-detector [22]. The physical mechanism of the NC behavior in different devices is obviously different. The phenomenon of NC behavior means that the material displays an inductive behavior. The observation of NC behavior is important because it implies that an increment in the bias voltage produces a decrease in the charge on the electrodes [5].

Many investigators have reported that an NC behavior can be observed in forward bias region [18], sometimes at high frequencies [22,23], sometimes at low frequencies [16] and sometimes at low temperatures [14]. According to Champness and Clark [12], the NC behavior, which is caused by the injection of minority carriers, can be observed only at forward bias and low frequencies. In practice, NC behavior can be explained on the basis of the behavior of the temperature and frequency dependent admittance spectroscopy (C–V and G/ω–V) data [13]. It is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, but detailed physical mechanism of the injection is not fully understood yet.

The origin of negative capacitance behavior in the forward bias C–V characteristics of Au/SiO_2/n-GaAs structures was investigated in a wide frequency range of 10 kHz–3 MHz at room temperature. In addition, the values of R_s, dielectric constant (ε'), dielectric loss (ε'') and loss tangent ($\tan\delta$) of these structures were obtained from C–V and G/ω–V measurements as a function of frequency and applied bias voltage.

2. Material and Methods

Au/SiO_2/n-GaAs structures were fabricated on the 5.08 cm diameter float zone (100) n-type GaAs wafer having thickness of about 350 μm with $2–3\times10^{18}$ cm^{-3} carrier concentrations. For the fabrication process, firstly the GaAs wafers were dipped in ammonium peroxide for a few seconds to remove native oxide layer on the surface. Au/Ge/Ni alloy was evaporated onto the whole back side of the wafer at a pressure about 10^{-7} Torr in a vacuum system. In order to perform the ohmic contact, wafer was sintered at 430 °C for 40 s. Insulator layer (SiO_2) was coated on the upper surface of the GaAs using 13.56 MHz rf power Plasma-Enhanced Chemical Vapor Deposition (PECVD) system. In PECVD system SiH_4 gas was used for Si source and O_2 gas for oxygen source. The O_2/SiH_4 ratio was kept at 1.3, while the SiH_4 gas flow rate and rf chuck power were held at 40 sccm and 100 W, respectively. The SiO_2 films were deposited at 150 °C whereas the process pressure was held fixed at 10 mTorr. The wafer was placed in the vacuum system, after front/Schottky contacts with a thickness of 1500 Å were formed at a rate of 2 Å/s by evaporating circular dots of high purity gold (Au) with 1 mm diameter through a metal shadow masks. The metal layer thickness and the deposition rates were monitored with the help of quartz crystal thickness monitor. The interfacial insulator layer (SiO_2) thickness was estimated to be about 240 Å from the measurement of the insulator capacitance (C_{ox}) in the strong accumulation region at 1 MHz.

The capacitance–voltage–frequency (C–V–f) and conductance–voltage–frequency (G/ω–V–f) characteristics of Au/SiO_2/n-GaAs structures were measured in the frequency range of 10 kHz–3 MHz at room temperature. The C–V and G/ω–V measurements were performed at different frequencies using HP 4192A LF impedance analyzer (5 Hz–13 MHz) and the test signal of 40 mV_{rms}.

3. Results and discussion

Many semiconductor devices, because of the metal contacts (rectifier, ohmic) and interfacial layers, have interface states and/or bulk traps in the structure. These interface states and/or bulk traps cause a large number of effects on the electrical and dielectric properties of the structure especially when the interfacial layer is thin [5,13]. This occurs because the interface states can follow the ac signal at lower frequencies and therefore yield an excess capacitance, which depends on the frequency. The voltage dependence of the C and G/ω at different frequencies (10 kHz–3 MHz) of the Au/SiO_2/n-GaAs structure is shown in Fig. 1(a) and (b), respectively. It is clear that the C–V and G_m/ω–V curves are quite sensitive to frequency at relatively high positive voltages; hence both the C–V and G/ω–V curves show frequency dispersion. For a given applied bias voltage in the positive region, C (up to the crosssection point) and G/ω values decrease with the increasing frequency because of the time-dependent response of the interface states. Also, each C–V curve gives a peak and the position of the peaks of C–V plots shifts towards reverse bias region with the increasing frequency and these peaks almost disappear at high frequencies. However, in the high frequency limit ($f\geq1$ MHz), the interface states cannot follow the ac signal. This makes the contribution of interface state capacitance to the total capacitance negligibly small [24–28].

As shown in Fig. 1(a), the values of C, which reach a maximum value at about 0.8 V, decrease rapidly with the increasing bias voltage in the forward bias region and take negative values after about 1.3 V. In the negative capacitance region, G/ω values continuously arise with the decreasing frequency while C values have more negative values. The reason of NC behavior has been investigated by some researchers [5,12,22,29]. Among those researchers, Jones et al. [5] explained this phenomenon with the relaxation material theory. According to Jones et al. relaxation material is responsible for NC behavior because of the injection of holes, which recombine easily with the electrons of the dipole near the junction and hence causes a decrease in the charge dipole. This mentioned process is strong and the charges involved are so close to the contact charges. Thus, the capacitance decreases with the increasing polarization and more carriers are introduced depending on the increments in polarization with the decreasing frequency; and the reverse