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Investigation of process parameter variation in the memristor based resistive random access memory (RRAM): Effect of device size variations

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ABSTRACT

The purpose of this work is to investigate the effect of device size and frequency on memristor based Resistive Random Access Memory (RRAM). The objects of investigation are effect on memory window, Low Resistance State (LRS) and High Resistance State (HRS) with memristor device size varied from 5 nm to 50 nm. Moreover, effect of device size variation on lifetime (τ) reliability of memristor device has also been explored. The results evidences that, memristor possess higher memory window and lifetime (τ) in the lower device size with lower frequencies. This subsequently consequences into lower data losses in the overall memory architecture having memristors as the basic building block. Authors have analysed effective variation in LRS and HRS by accomplishing Monte-Carlo simulation. The results of Monte-Carlo simulation suggests the LRS to follow Weibull distribution whereas HRS to go along with Gaussian distribution for less read and write errors.

1. Introduction

With the symmetry arguments in place, memristor has been regarded as the fourth circuit element along with resistor, inductor and capacitor [1]. Memristor exhibits a unique property of maintaining relationship between the time integrals of current and voltage across its terminals which enables it to remember the last functional state in the form of current or voltage. The two fold significant potential of the memristor viz. as basic building blocks of logic gates as well as for storage have revealed them as promising constituents in realisation of silicon photonic computers.

The literature survey reveals that the memristors have been developed using Metal/Insulator/Metal (MIM) structure which leads to bipolar or unipolar resistive switching effects [2,3]. The bipolar resistive switching memories have two distinct resistance states viz. Low Resistance State (LRS) and High Resistance State (HRS). Accordingly data can be stored in terms of these states, for instance the Low Resistance State (LRS) corresponds to logic '1' while the High Resistance State (HRS) to logic '0'.

Good number of research groups are working on Memristor based Resistive Random Access Memory (RRAM) implementations. Recently Murali et al. reported memristor based RRAM using zinc–tin-oxide (ZTO). Superior switching ratio, long retention time, and good endurance in developed memory device are the key features of the above referred

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development [4]. As discussed by Chang et al. the above key features along with the transition of short-term memory to long-term memory in a memristor makes them promising elements for biological applications [5]. In nutshell many researchers are striving hard to come out with improved memristor device by following different synthesis routes for superior metrics in light of their applications for RRAMs. The research group of Marjanović et al. has done work both from device making and simulation in context with improving the metrics of the memristors [6–8]. They studied the effects of exposing heavy ion beams on TiO_2 memristors. Their study reveals that the exposure of heavy ions reduces the resistance of memristor and mobility oxygen vacancies. This leads to lowering the state retention ability of the memristor device [6–8]. Younis et al. discussed the novel way to improve the resistive switching performance using quantum dots as surface charge trappers [9]. Dongale et al. reported the TiO_2 thin film memristor with low symmetric voltage switching [10].

In continuation of above, our work presented in this paper investigates the effect of device size and frequency on memory window, LRS and HRS of memristor based Resistive Random Access Memory (RRAM). The life time of the device has been probed using the above referred analysis. The details of this paper are as follows. After brief introduction in the first section, Sections 2 and 3 deal with the simulative investigation of effect of device size and frequency on memristor based RRAM. Furthermore, effect of device size and frequency variation on lifetime (τ) reliability of memristor device is examined in Section 4. The results evidences the memristor developed herein embodies higher memory window and lifetime (τ) in the lower device size with lower frequencies. This signifies lower data losses in the memory architecture. Monte-Carlo simulation has been undertaken to present the effective variations in LRS and HRS.

2. Simulation framework

The memristor properties have been simulated herein according to HP memristor model [11]. The basis for the same is Eq. (1) wherein the device size (D) has been varied from 5 nm to 50 nm with increase in frequency specifically 1, 2, 4, 10, 100 and 200 Hz. The subsequent effect on various properties have been observed and presented in the rest of the paper.

$$M(q) = R_{OFF}\left(1 - \frac{\psi \mu_v R_{ON}}{D^2} q(t)\right) \quad (1)$$

For the present simulation following parameter values have been fixed. Input sinusoidal signal- V_M sin wt, where $V_M = 1$ V, frequency of applied signal = 1, 2, 4, 10, 100, and 200 Hz, D = 5–50 nm, w = 2, 4, 6….20 nm for each D; M-efficiency factor kept as 200 for each simulation trial with $\psi = 1$. Outcome of the simulation has been discussed in the following section.

3. Effect of frequency and device size on memristor based RRAM

At the outset the results are reaffirming the fact that the memristance is a truly nanoscale phenomena and characteristics of memristor are significantly gets improved as the device dimension shrinkages to nanoscale. In the HP mem-

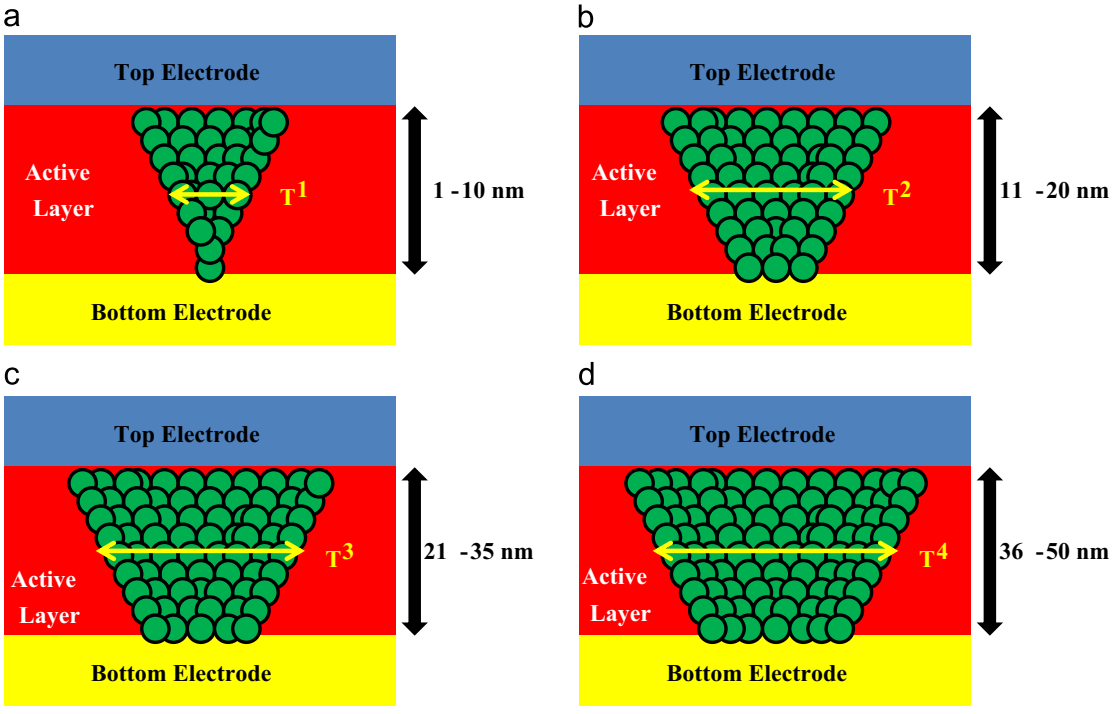

Fig. 1. (a–c): LRS and HRS variations with respect to device size. (a) Represents conduction filament at lower device size (5–10 nm). (b)–(d) Represent conduction filament at higher device size (11–20 nm, 21–35 nm and 36–50 nm respectively).