Materials Science in Semiconductor Processing 26 (2014) 506–511

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Simulation analysis of a novel dual-trench structure for a high power silicon-on-insulator metal–semiconductor field effect transistor

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ARTICLE INFO

Available online 5 June 2014

Keywords:
Breakdown voltage
Dual-trench
Silicon-on-insulator
MESFET

ABSTRACT

In this paper, a silicon-on-insulator (SOI) metal–semiconductor field-effect transistor (MESFET) by a novel dual-trench technique is presented. In the proposed technique, the dual-trench is created in the buried oxide and filled with p-type and n-type doped Si. The p-type trench beneath the source increases breakdown voltage (V_{BR}). Also, the n-type trench beneath the gate improves the drain current (I_D). We call this new structure as Dual-Trench SOI MESFET (DT-MESFET). DC and radio frequency (RF) characteristics of the proposed structure are analyzed by 2-D numerical simulation and compared with conventional SOI MESFET (C-MESFET) characteristics. The extracted results show that the dual-trench technique has excellent effect on I_D, V_{BR}, and maximum output power density (P_{max}) of the device. The parameters, V_{BR}, I_D, and P_{max} of the DT-MESFET structure are improved by 55.55%, 50%, and 300% compared with those of the C-MESFET structure, respectively. Also, the dual-trench technique leads to the enhancement of maximum oscillation frequency and maximum available gain. Therefore, the novel SOI MESFET structure has superior electrical characteristics as compared to the similar device based on the conventional structure.

1. Introduction

Field effect transistors are classified as metal semiconductor field effect transistor (MESFET) and high electron mobility transistor (HEMT or MODFET). Due to presence of large capacitance formed by gate electrode and the insulator in MESFETs, it is utilized in relatively low and medium frequency applications. MESFET and HEMT present high frequency applications more than 70 GHz [1–4].

Regarding to HEMT structure, HEMT is a field effect transistor incorporating a junction between two materials with different band gaps. The frequency of HEMT is almost 100 times faster than MESFET [2]. But, fabrication process of the MESFET structure is easiest than HEMT structure because the MESFET structure do not include various materials.

Nowadays, silicon-on-insulator (SOI) technology attracts much attention in high-speed and low-power consumption applications. SOI structures have important advantages such as low junction capacitance, latch-up immunity, and improved device isolation due to using the buried oxide (BOX) [5,6]. Also, metal–semiconductor field-effect transistor (MESFET) is considered as promising candidate for high-power applications in military communications, telecommunication cellular base stations, satellites, aerospace, and data storage [7,8]. MESFETs which are made based on the SOI

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http://dx.doi.org/10.1016/j.mssp.2014.05.040
1369-8001/

technology (SOI MESFET) have attractive features, such as operation capability in the high frequency making it suitable for various electrical applications [9].

Mentioned issues above cause wider band width, lower the size and reduced weight of systems. In spite of lower electron mobility of silicon with respect to GaAs, good microwave performance can be obtained with submicron gate devices that their saturation velocity is nearly double that in GaAs. However, short channel length coupled with larger drain voltage in the MESFETs will result in short channel effects such as the drain induced barrier lowering (DIBL) effect, thus degrading the device performance in a form of threshold voltage shift and high output conductance.

In order to improve the DC and RF characteristics of the conventional Si MESFET, we have introduced a new dual-trench technique. In the proposed technique, the dual-trench is created in the buried oxide and filled with p-type and n-type doped Si. The n-type trench beneath the gate and also the p-type trench beneath the source improve the drain current (I_D) and breakdown voltage (V_{BR}) of the proposed structure. We called this new structure as Dual-Trench SOI MESFET (DT-MESFET). By two-dimensional and two-carrier device simulation [10], we have investigated the DC and RF characteristics of proposed structure and compared it with a conventional SOI MESFET (C-MESFET) structure. The numerically obtained results show that our structure can be considered as a candidate to replace the conventional SOI structure.

2. DT-MESFET structure and simulation method

Fig. 1 shows the schematic cross-sectional view of the DT-MESFET structure consisting of two trenches located in the buried oxide. The trenches are created in the buried oxide beneath source and gate regions and filled with p-type and n-type doped Si. The DT-MESFET structure dimensions are as follows: The drain and source lengths are 0.3 μm, gate length L_G=0.5 μm, gate–drain spacing L_{GD}=0.5 μm, and gate–source spacing L_{GS}=0.5 μm. Also, the p-type substrate layer has a thickness of 0.1 μm and the doping level of 1×10^{13} cm^{-3}. The BOX region thickness is set to 0.4 μm and the n-type active layer is doped at 1×10^{17} cm^{-3} with a thickness of 0.2 μm. The n-type cap layer doping level is 1×10^{20} cm^{-3}. As Fig. 1 shows, the dimensions of both the trenches are equal. After optimization considerations on the dual-trench dimensions, the

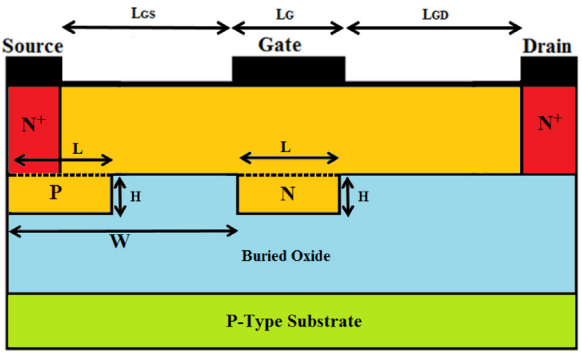

Fig. 1. Schematic cross-sectional view of DT-MESFET structure.

Table 1
Typical parameters for the DT-MESFET structure.

Parameter	Value
Gate length (L_G)	0.5 μm
Drain length (L_D)	0.3 μm
Source length (L_S)	0.3 μm
Gate-drain spacing (L_{GD})	0.5 μm
Gate-source spacing (L_{GS})	0.5 μm
p-Type substrate layer thickness	0.1 μm
p-Type doping level	1×10^{13} cm^{-3}
BOX region thickness	0.4 μm
n-Type active layer doping level	1×10^{17} cm^{-3}
n-Type active layer thickness	0.2 μm
n-Type cap layer doping level	1×10^{20} cm^{-3}
Length of dual-trench (L)	0.5 μm
Height of dual-trench (H)	0.1 μm
Doping density of dual-trench (N_T)	1×10^{17} cm^{-3}

length (L) 0.5 μm, and height (H) 0.1 μm are achieved for the trenches. The doping densities at both the trenches are identical and equal to $N_T=1\times10^{17}$ cm^{-3}. The spacing between the n-type trench and the device left end (W) is 0.8 μm. It is worth noting that the conventional SOI (C-SOI) MESFET parameters are equal to those of the DT-MESFET without the dual-trench regions. Parameters for the proposed structure are listed in Table 1. It is worth noting that typical structural parameters of the proposed structure have been selected according to the paper [11].

We propose a process flow for the fabrication of the DT-MESFET. The fabrication process starts with one p-type ⟨1 0 0⟩ oriented silicon wafer called “wafer A” and one n-type ⟨1 0 0⟩ oriented silicon wafer named “wafer B”, which can be seen in Fig. 2(a). As shown in Fig. 2(b), a thermal oxide can be grown on the wafer A. Then, a via is defined in the oxide layer (Fig. 2(c)) and then n and p type silicon layer deposition is done. This type of deposition is the chemical vapor deposition (CVD) (Fig. 2(d)). As shown in Fig. 2(e), the surface oxide is removed by a CMP process to eliminate the residual defect region over the oxide. Fig. 2(f) shows that wafer B which is bonded to support wafer A by wafer bonding. Finally, the fabrication process will be completed in Fig. 2(g).

In order to simulate the devices accurately, Atlas that is a 2-D simulator from SILVACO with silicon based and impressive physical models is utilized. To get true and precise results, the basic Poisson and drift–diffusion equations and also the other impressive physical models including SRH (Shockley–Read–Hall), Auger, Arora, BBT. std, Analytic, CVT, BGN, Fldmob, Conmob, Incomplete, and Impact Selb are activated in the simulator.

It is important to mention that the simulator is calibrated with experimental data in the micrometer regime [12]. Fig. 3 shows the comparison of the drain current versus drain voltage for the experimental data and simulation results. The figure makes sure that the ATLAS simulator is really an accurate semiconductor device simulation tool.

3. Results and discussions

This section presents the extracted results by ATLAS simulator for both the structures. Main characteristics such