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N^+ plasma-assisted wafer bonding between silicon and chemical vapor deposition oxide at low temperature

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ABSTRACT

Room-temperature bonding between low-pressure chemical vapor deposition (LPCVD) oxide and silicon has been achieved by using N^+ plasma activation and chemical mechanical polishing (CMP). The bonding energy reaches the value of bulk silicon fracture energy (about 2.5 J/m^2) after annealing at 400 °C for an hour, which is higher than the bonding energy between thermal oxide and silicon using the same process. The density difference is believed to be the main contributor to the enhanced bonding energy. Silicon-on-insulator (SOI) substrate is fabricated using Smart-Cut technology and then chemical mechanically polished to obtain a reasonably smooth surface for device manufacture. This low-temperature bonding process can be used in many applications, such as microelectromechanical systems (MEMS) and three-dimensional integration.

1. Introduction

Wafer bonding refers to the bonding between two mirror-polished, flat and clean wafers; the contacting force consists of Van der Waals force and hydrogen bond. It has become a key technology in many applications ranging from microelectronic devices based on SOI material to MEMS devices manufacture and packaging [1]. Chemical mechanical polishing (CMP) process can remove material from uneven topography on a wafer surface until a flat surface is obtained. Nowadays, CMP has been applied mainly in the interconnect structure of the integrated circuit (IC) chip fabrication. The combination of wafer-bonding technology and CMP process has led to a widening use of wafer bonding [2,3].

Tan et al. [2] have studied low-temperature direct bonding between polished plasma-enhanced chemical vapor deposition (PECVD) oxide and thermal oxide. They achieved void-free bonding interface and obtained the bonding strength of 432 mJ/m^2 after annealing at 300 °C for 6 h. However, this bonding strength is too weak to withstand the following manufacturing steps. Furthermore, the annealing time is too long and limits its application to thermal-sensitive materials. Suni et al. [3] have presented an available process for wafer-scale packaging of MEMS using plasma-activated wafer bonding and back-grinding technology. The wafers were plasma activated in an inductively coupled plasma chamber (ICP) with 30 s argon plasma treatment. Unfortunately, the ICP will inevitably cause metal-ion contamination on the wafer surface, which is not compatible with the IC fabrication and the grind-back process takes long to attain the top thin Si film.

In our experiment we used N^+ plasma-activation-based bonding process, which can both enhance the

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bonding strength and shorten the annealing time. The plasma activation was achieved using a special chamber, which was coated with a thin silicon film from inside. It can decrease metal-ions contamination and is compatible with thin SOI substrate manufacturing [4]. The bonding-energy measurement shows that the bonding strength between the LPCVD oxide and silicon is much higher than that between thermal oxide and silicon after low-temperature annealing. High-quality silicon on LPCVD oxide (SOI) structure was fabricated using CMP process and Smart-Cut technology. After the final CMP process, the root-mean-square (rms) surface roughness of top silicon was reduced from 10 to 0.85 nm (scan size $5\,\mu m \times 5\,\mu m$). The surface smoothness enables three-dimensional (3D) integration of microelectronic devices and potential integration of optoelectronic devices. We have recently proposed a 3D CMOS integration method, which is based on the CVD deposited oxide and Si wafer bonding [5]. In such a 3D CMOS scheme, the PMOS and NMOS circuits are fabricated in respective Si layers with deposited oxide layer in between. To realize the scheme, the hydrogen-implanted Si wafer is bonded to an NMOS device wafer face to face. In the following annealing process, a thin Si film, on which PMOS is to be fabricated afterwards, is transferred onto the device wafer. Because the NMOS device wafer has gone through the N-type source/drain-doping process, it is important to control the thermal budget to prevent dopant redistribution. Thus, both the subsequent annealing temperature and time should be carefully controlled. Finally, a high bonding energy, which is strong enough to keep the top Si layer intact during subsequent CMP process, is obtained after annealing at 400 °C for an hour.

2. Experimental details

In our experiments, p-type 3-in silicon (1 0 0) wafers with the resistivity of 10–20 Ω cm were used. Three kinds of wafers including silicon wafers with 1200-nm-thick LPCVD deposited oxide layer, silicon wafers with 800-nm-thick thermal oxide layer and bare silicon wafers were prepared. One of the silicon wafers was implanted with H^+ at 140 keV at a dose of $6 \times 10^{16}/cm^2$. Since the surface of as-deposited LPCVD oxide is rough (the rms roughness is much larger than 1 nm), CMP process was used to flatten the surface. The equipment is a CMP Tester (CETR CP-4) with an IC 1000/Suba IV stacked pad (Rodel). Polishing parameters were as follows: pad rotation speed 150 rpm, wafer rotation speed 147 rpm, down force 3 psi, feed rate of the slurry 100 mL/min.

Then all of the wafers were cleaned in a modified Radio Corporation of America 1 (RCA1) and RCA2 solution [6], and dried. The surface of all the wafers was then activated by N^+ plasma in a newly developed setup (EVG810 low-temperature plasma-activation system) for 20 s. The plasma was ignited between two parallel electrodes. The process pressure was 0.4 mbar, the top/bottom electrode power was 100/75 W. The special chamber of EVG810 can not only prevent any potential surface damage during the plasma exposure but also decrease the metal-ion contamination to the surface [4]. After surface activation the wafers were cleaned using de-ionized (DI) water and megasonic water successively. Afterwards the LPCVD oxide wafer and thermal oxide wafer were bonded with silicon wafers, respectively. The bonding process was accomplished at room temperature (RT) in air in a "Class 1" micro-clean room integrated in the EVG301. An infrared (IR) imaging system was used to investigate the bonding interface. After bonding, samples were annealed at 200, 300, 400, and 500 °C for an hour, respectively. The bonding energy of the as-bonded samples and annealed samples was measured by the well-known crack-opening method [7]. A blade was inserted into the interface of the bonding pair at a fixed velocity. By measuring the crack length, the bonding energy was determined. The experimental error associated with the crack-opening measurement is typically about ±15% depending on the accuracy of the crack lengths L measured. Bonding pairs

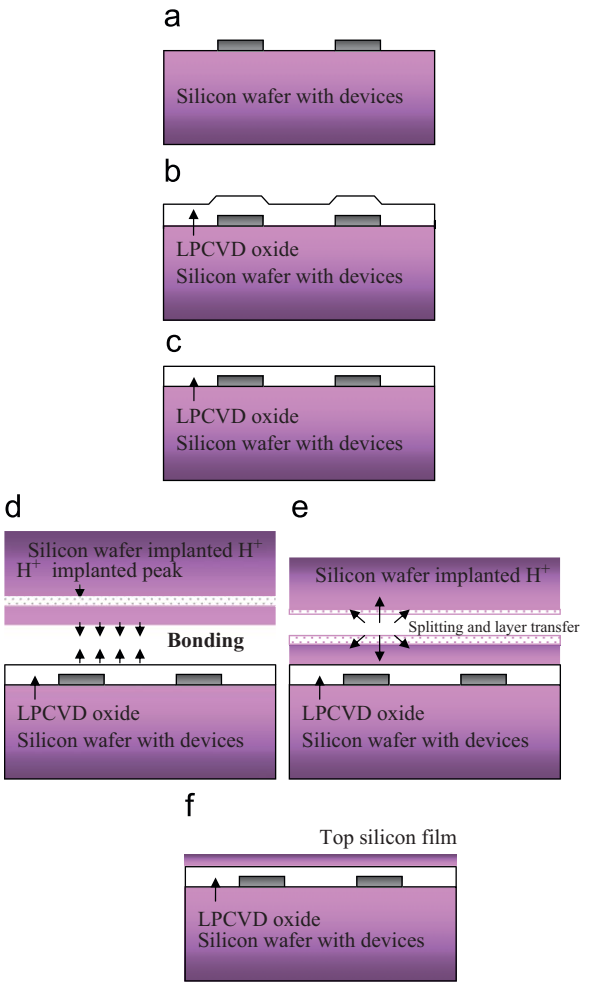

Fig. 1. Process flow of plasma-assisted wafer bonding using CMP process: (a) start handle wafer, (b) LPCVD oxide deposition, (c) oxide surface smoothness using CMP, (d) N^+ plasma-assisted wafer bonding of hydrogen-implanted Si wafer to handle wafer, (e) heat treatment of bonded pairs and Si-film transfer, (f) final CMP to smoothen the top silicon surface.