Available online at www.sciencedirect.com
ScienceDirect
Materials Science in Semiconductor Processing 9 (2006) 721–726
MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING

1/*f* noise performance of MOSFETs with HfO_2 and metal gate on Ge-on-insulator substrates

P. Srinivasan[a,b], E. Simoen[a,*], B. De Jaeger[a], C. Claeys[a,c], D. Misra[b]

[a]*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*
[b]*Department of Electrical and Computer Engineering, NJIT, Newark, NJ, USA*
[c]*E.E. Department, KU Leuven, Belgium*

Available online 20 September 2006

Abstract

The low frequency (1/*f*) noise performance of *n*- and *p*-MOSFETs with HfO_2 and TiN–TaN metal gate on GeOI substrates has been investigated. The LF noise spectra are of the $1/f^{\gamma}$ type, with $\gamma > 1$. The current noise spectral density is typically one decade higher than for silicon counterparts. The behavior of the noise characteristics points to carrier trapping as the prevailing 1/*f* noise mechanism. Using a tunneling coefficient $\alpha = 6.5 \times 10^7\,cm^{-1}$ for the Ge/HfO_2 system, the extracted volume and surface trap densities are in the range of $1 \times 10^{20}/cm^3\,eV$ and a few $10^{12}/cm^2$ respectively. This is of the same order as the interface trap densities, obtained from charge pumping. It is believed that the Ge/interfacial layer (IL) quality could be responsible for the significantly higher trap densities and noise, compared with Si/HfO_2/ TiN–TaN MOSFETs.

Keywords: HfO_2; Germanium; Low-frequency noise; Metal gate; Number fluctuations; Tunneling coefficient; Interface traps

1. Introduction

Original MOS development took place on germanium substrates and the first studies on 1/*f* noise in MOSFETs happened on Ge, leading in the 50-ties to the McWhorter theory on 1/*f* noise [1]. This model is still frequently used to explain the noise behavior. Currently, the fundamental limits imposed by down-scaling of transistors for the sub-45 nm node puts Ge back on the microelectronics scene, one of the main reasons being the strong improvement of low-field electron and hole mobility compared with silicon [2]. Encouraging results were obtained by several groups in the development of CMOS on Ge [3–6]. Recently, the good device performance of Ge *p*-MOSFETs with PtSi Schottky-barrier germanide source/drain and HfAlO gate dielectric and HfN–TaN electrodes has been reported [7]. It is the aim here, to close the circle started in the 50s and to present initial results of a LF noise characterization on state-of-the-art Ge-on-insulator (GeOI) MOSFETs with HfO_2 gate dielectric (equivalent oxide thickness–EOT–2.7 nm) and TiN–TaN metal gate, fabricated in a ULSI silicon compatible process flow. As will be shown, mostly 1/*f*-like spectra have been observed, which can be understood in the frame of the McWhorter or number fluctuations theory. Compared with

*Corresponding author. Tel.: +32 16 281 381; fax: +32 16 281 706.
E-mail address: simoen@imec.be (E. Simoen).

1369-8001/$ - see front matter © 2006 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mssp.2006.08.018

TiN–TaN/HfO_2 devices on a silicon substrate, a 1–2 orders of magnitude higher current noise spectral density (S_{id}) is observed, from which a higher density of oxide traps (D_t) is derived. The latter is in reasonable agreement with the interface trap density (N_{it}) derived from charge-pumping measurements on similar devices.

2. Experimental

Processing was performed on 200 mm diameter GeOI substrates fabricated by the smart-cut process, as described elsewhere [8]. The silicon-like process flow used to fabricate the Ge devices is outlined in [6]. The gate dielectric stack process consists of several steps [9]. The wafers were first dipped in an HF-2% solution followed by a pre-bake step in H_2 to remove the native oxide from the Ge surface. A thin layer (~0.46 nm) of epitaxial Si was grown on the surface and was partially oxidized in a N_2O plasma at room temperature to form a thin SiO_2 interfacial layer (IL). Next, 10 nm HfO_2 was deposited on top of the IL by atomic layer deposition (ALD) at 300 °C. A TaN metal gate was made by physical vapor deposition (PVD), on top of which a PVD TiN capping layer was deposited. Post-deposition annealing (PDA) was carried out in an O_2 environment at 400 °C for 1 min. The thickness and doping density of the Ge layers were such that the fabricated transistors are partially depleted. XPS measurements showed that the equivalent oxide thickness (EOT) of the formed interfacial SiO_2 layer was 0.65 nm. The total EOT of the gate stack was 2.7 nm based on standard C–V measurements. Fig. 1 shows a TEM picture of the device without the metal gate formation.

$W/L = 10/1\,\mu m$ n- and p-channel Si/HfO_2/TaN–TiN devices were also fabricated using a conventional CMOS process flow. In this case, a 0.8 nm thin IL obtained by an ozone treatment was first formed on top of which HfO_2 was deposited by a metal organic chemical vapor deposition (MOCVD) process. The devices underwent decoupled plasma nitridation (DPN), similar to the N_2O treatment received by the Ge devices before the deposition of the metal electrode. The same TiN–TaN metal gate was deposited by PVD. These devices were post-deposition annealed in NH_3 at 800 °C for 60 s, followed by annealing in forming gas (FGA) at 520 °C for 20 min. The equivalent oxide thickness of the silicon transistors was estimated to be 2 nm.

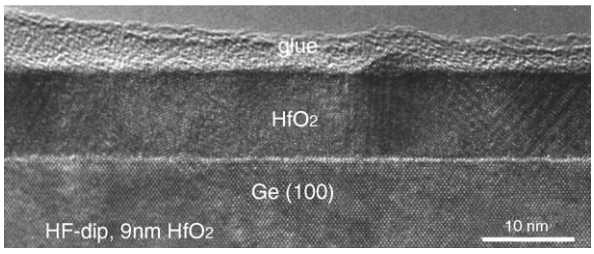

Fig. 1. TEM photograph of a HfO_2 dielectric on a GeOI substrate, without the metal gate formation.

The treatment of the IL of the Ge devices is certainly different when compared to the Si counterparts, mainly due to the lower stability of GeO_2 compared with SiO_2. It has been shown earlier [9] that for the same conventional silicon-like CMOS process flow, the formation of an IL by an ozone-based process on GeOI substrates resulted in higher interface trap densities, which for sure will lead to much higher noise. For Si devices, it has also been demonstrated that the deposition technique (ALD vs. MOCVD) has no strong impact on the interface state densities in the high-k layer, though a variation in noise mechanism is observed [10,11]. However, as will be shown here, the best interface engineering on GeOI available today still results in a significantly larger $1/f$ noise.

On-wafer noise measurements were performed in linear operation at a constant drain voltage $|V_{ds}| = 0.05$ V for gate voltages $|V_{gs}|$ between 0.5–2 V, in steps of 50 mV using a BTA9812 noise analyzer and NoisePro software from Cadence. A channel length of 1 μm was chosen for both the Si and Ge substrate devices, to reduce device-to-device scatter in the noise magnitude.

3. Results and discussion

Fig. 2 shows the transfer characteristics of both p- and n-MOS for $|V_{ds}|$ of 1 V. The corresponding threshold voltage V_t is ~1.5 V (n-MOS) and ~−0.5 V (p-MOS). A high off-state leakage current is observed for n-MOS, which is attributed to non-optimized dopant activation conditions, resulting in residual ion implantation damage in the depletion region of the substrate-drain junction [6].

Fig. 3(a) shows LF noise spectra of n-MOSFETs processed on both Si and Ge substrates. A scaling of the V_{ds} has been taken into account, and the gate voltage overdrives $|V_{gs}–V_t| = 1$–1.5 V. The noise performance of the p-MOSFETs is shown in Fig. 3(b).