Materials Science in Semiconductor Processing 30 (2015) 41–47

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Investigation of impact ionization and flicker noise properties in indium aluminum arsenide/indium gallinum arsenide metamorphic high electron mobility transistors with various work function-gate metals

Hsien-Chin Chiu [a,*], Chia-Hsuan Wu [a], Che-Kai Lin [a], Feng-Tso Chien [b]

[a] Department of Electronics Engineering, Chang Gung University, Taoyuan, Taiwan, ROC
[b] Department of Electronics Engineering, Feng-Chia University, Taichung, Taiwan, ROC

ARTICLE INFO

Available online 31 October 2014

Keywords:
MHEMT
Flicker noise
Impact ionization
Kink effect

ABSTRACT

This study investigates the effect of impact ionization using Ir, Pt, Pd, Ti gate metals and the direct correlation between these high work function metals and low frequency noise (LFN) on an $In_{0.4}Al_{0.6}As/In_{0.4}Ga_{0.6}As$ metamorphic high electron mobility transistor (MHEMT). The effect of impact ionization on DC, RF, and cryogenic LFN is systematically studied and discussed. Gate metals with high work functions are used to suppress the kink effect and gate leakage current. Experimental results suggest that the Ir gate MHEMT exhibits superior thermal stable properties in a strong electrical field at various temperatures, associated with high gain, high current, and excellent low-frequency noise performance.

1. Introduction

As the scaling down of silicon based devices reaches its limit, III–V compound semiconductor field effect transistors have been identified as some of the most attractive nanoelectronic devices [1–3]. In particular, InP-based high electron mobility transistors (HEMT) exhibit high power, high operating frequency, low distortion, and low noise characteristics [4–7]. These are favorable for millimeter wave applications. A high indium content in a channel layer generally corresponds to high electron mobility and velocity, making InAs channel hetero-structured FETs (HFETs) highly suitable for low-power and high-speed logic applications, since they have an extremely high electron mobility of more than 30,000 $cm^2/V\,s$ [8,9]. However, the narrow bandgap of an InGaAs channel with high indium content clearly has a negative effect on impact ionization. In a strong electric field beneath the gate depletion region, the "highly energetic" electrons and holes in the conduction or valence band can collide with each other, creating electron–hole pairs, which are excited to the conduction band. Impact ionization further induces the kink effect, which is a sudden rise in the drain current at a certain drain-to-source voltage that causes high drain conductance and transconductance (*Gm*) compression, leading to reduced voltage gain and yielding linearity [1,10]. The kink effect corresponds to Schottky characteristics. Gate metal stacks strongly dominate the device performance, including threshold voltage, *Gm*, gain, and reliability. Most importantly, the use of gate metals with a high work function can limit the kink effect and the gate leakage current.

The metals that have previously been studied as gate metals include Ti [11–14], Pt [15–17] Pd [11,12,18], and Ir [19–21]. Pt exhibits the highest SBH (Schottky barrier height) ≥ 0.8 eV on InAlAs, and has been widely used for the

* Corresponding author. Tel.: +886 3 2118800; fax: +886 3 2118507.
E-mail address: hcchiu@mail.cgu.edu.tw (H.-C. Chiu).

http://dx.doi.org/10.1016/j.mssp.2014.09.035
1369-8001/

enhanced mode HEMT process. However, during the production or thermal treatment of process baking, gates with incorporated Pt suffer from severe diffusion problems, further influencing the characteristics and reliability of the devices [16]. A thermally stable gate metal is urgently required. Recent investigations revealed that iridium is a promising gate metal. Ir gates have a similar SBH to those of Pt gates on InAlAs epi-layers and exhibit a lower diffusion rate and greater thermal stability than Pt on InAlAs [22]. This investigation examines the kink effect associated with gate metals with high work functions and it has direct correlation with low frequency noise (LFN). The total effects of impact ionization on DC, RF, and cryogenic LFN will be systematically studied and discussed.

2. Device fabrication and structure

Fig. 1 presents a cross-sectional photograph of the MHEMT with an epitaxial structure, grown on GaAs substrate. The grown wafers comprised of a 1 μm thick $In_xAl_{1-x}As$ metamorphic graded buffer layer with an indium content grading of $x=0$–40%. Two two-dimensional electron gases formed in this $In_{0.4}Ga_{0.6}As$ quantum well and electrons were transferred from both upper and lower silicon δ-doped layers through undoped $In_{0.4}Al_{0.6}As$ spacer layers. The 150 Å thick $In_{0.4}Al_{0.4}As$ Schottky layer sits on top of the upper Si δ-doped layer to increase the height of the Schottky barrier, and a 100 Å-thick un-doped $In_{0.52}Ga_{0.48}As$ cap layer was grown to enhance ohmic contact resistivity. The designed structure had a sheet-charge density of $3.5\times10^{12}\,cm^{-2}$ and a Hall mobility of $8500\,cm^2/V\,s$ at 300 K after the un-doped $In_{0.52}Ga_{0.48}As$ cap layer was removed. For device fabrication, low-resistivity ohmic contacts of Ni/Ge/Au alloy metals were deposited by thermal evaporation and patterned using a conventional lift-off process, followed by annealing at 320 °C in an N_2-rich chamber for 20 s. A chemical etching method was utilized for the mesa isolation. The drain-to-source spacing was set to 3 μm to minimize series resistance. Following the highly selective chemical gate recess process, $2\times50\,\mu m^2$ Ir/Ti/Au (10 nm/20 nm/200 nm), Pd/Ti/Au (10 nm/20 nm/200 nm) and Pt/Ti/Au (10 nm/20 nm/200 nm) gate stacks were deposited and lifted off. After evaporation of the Ti/Au interconnection, a 20 nm-thick layer of SiO_2 was deposited for passivation. For comparison, a conventional Ti/Au gate was also fabricated.

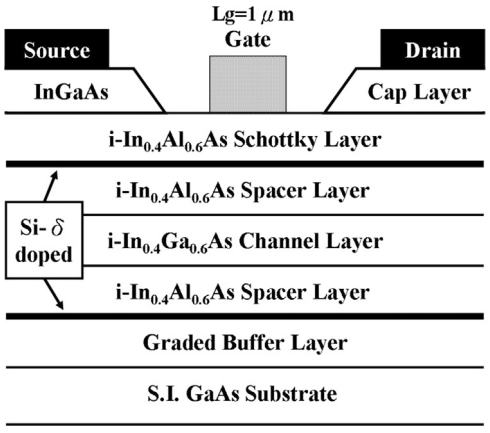

Fig. 1. Cross-sectional structure of the fabricated MHEMT.

3. Measurement results and discussion

Fig. 2 plots the DC characteristics of devices with a gate length of 1 μm and Ir, Ti, Pd, Pt gate MHEMTs at room temperature. Notably, the drain currents of the Ir gate MHEMT show a good output *I–V* characteristics. In contrary, Pd and Pt gate MHEMTs increase at a constant rate with drain-to-source voltage (V_{DS}) > 1 V. Ti gate MHEMT has the worst drain current. The humping curves are direct evidence of impact ionization. Fig. 3 plots the dc transconductance (*Gm*) versus gate-to-source voltage (V_{GS}) at various V_{DS} from 0.5 to 3 V. At $V_{DS}=1$ V, the Gm_{max} values of Ir, Ti, Pt, and Pd gates are 335, 372, 367, and 370 mS/mm, respectively. However, as V_{DS} increases, the impact ionization that is caused by the increasingly strong electric field becomes severe. The generation of electrons in the channel enhances both I_{DS} and *Gm*. Generated holes are collected at the gate terminal, causing a negative shift of V_{GS}. From Fig. 3, Ti and Pd gate MHEMTs suffered greater impact ionization than did Ir and Pt gate MHEMTs. Fig. 4 plots the

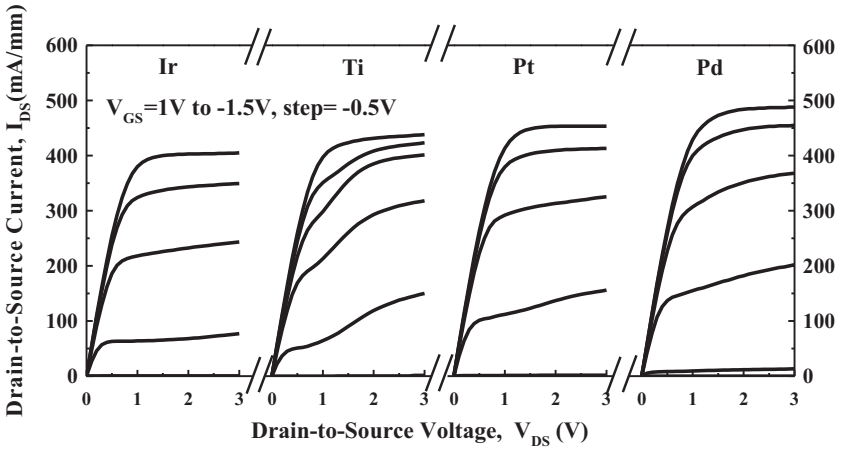

Fig. 2. The I_{DS}–V_{DS} characteristics of various devices.