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Rapid thermal annealing of cerium dioxide thin films sputtered onto silicon (111) substrates: Influence of heating rate on microstructure and electrical properties



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ABSTRACT

The impact of the heating rate (HR) of a Rapid Thermal Annealing (RTA) on the crystallinity and on the morphology of CeO_2 thin films has been investigated by Raman Spectroscopy (RS), Photoluminescence (PL), Scanning Electron Microscopy (SEM), Energy Dispersive Spectroscopy (EDS), and tapping mode Atomic Force Microscopy (AFM). The electrical properties of CeO_2 thin films have also been studied with the Conductive AFM mode. This paper highlights the importance of the heating rate value used during an RTA on crystalline quality, morphology and on the electrical properties of the CeO_2 layer. In fact, the best crystallinity with a good morphology and a high resistivity has been obtained for a CeO_2 layer sputtered on (111) Si substrate and post-annealed at 1000 °C for 30 s with an HR of 25 °C/s.

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1. Introduction

The epitaxial growth of cerium oxide films on silicon substrates has been studied for various applications in microelectronics [1–10], such as storage capacitors in Dynamic Random Access Memory devices. Furthermore, Resistive Switching in CeO_x films are interesting for Nonvolatile Memory Application. In fact, Sun et al. highlighted that CeO_x based Resistance Random Access Memory devices show uniform reset/set voltages, distinct High Resistance State and Low Resistance State resistances, and current compliance

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http://dx.doi.org/10.1016/j.mssp.2014.10.010 1369-8001/© 2014 Elsevier Ltd. All rights reserved. free bipolar Resistive Switching behaviors [11]. The multilevel intrinsic resistance states of CeO_x observed could be attributed to the separated line-pattern oxygen-vacancy distributed in the CeO_x films [11]. The role of oxygen vacancies for the resistance switching effect in cerium oxides has also been reported by Gao et al. [12]. Cubic fluorite CeO₂ has an excellent lattice matching with silicon (misfit factor of 0.35%), so it is expected to be one of the promising buffer layers that combine silicon and various oxides exhibiting superior properties such as high-Tc superconductivity [1,13] or ferroelectricity [14]. Also, due to its relatively high dielectric constant (≈ 26), CeO₂ was known to be a good candidate as the ultra-thin gate-insulating layer on Si, which was expected to enable the scaling down of the silicon based devices [15–17]. Recently, cerium oxide has drawn a lot of

attention, because of its technological importance in catalysis [18]. The possibility of the reversible transition from CeO_2 to Ce₂O₃ makes cerium oxide one of the promising materials, the desired catalytic properties of which can be adjusted by a suitable choice of metal or metal oxide additives. In fact, the substitution of a part Ce⁴⁺ by other suitable cations improves the low temperature reducibility and the oxygen storage capacity of cerium oxide [19]. However, CeO₂ may also be useful for radiation dosimeters [20,21] because nuclear radiations modify the electrical conductivity of CeO₂ film structures. Moreover, the cerium oxide film has potential applications in optical, electro-optical, and optoelectronic devices [22]. This oxide has even been used as a non-radioactive surrogate for UO₂ because its cubic fluorite-type structure is the same as UO₂ and it exhibits a similar defect evolution under irradiation [23].

In the literature, textured CeO_2 layers can be made using different growth methods like pulsed laser deposition [24,25], ion beam assisted deposition [26], rf sputtering [27,28], dc sputtering [29], e-beam evaporation [30], metal organic chemical vapor deposition [31], plasma enhanced chemical vapor deposition [32], spray pyrolysis [33], molecular beam epitaxy [34], and sol–gel process [35].

Some papers showed that a high growth temperature [25] and a post-deposition rapid thermal annealing [36] allowed to improve the crystalline quality of the CeO_2 films grown on (111) Si substrate.

Most of the time, studies focused on the influence of thermal annealing highlight the impact of the annealing time and temperature on the crystalline quality [37,38] and electrical properties [39] of the CeO₂ layers. Besides, we have also shown in a previous paper, that the best crystalline quality of CeO₂ layers deposited on a (111) Si substrate was obtained for an RTA performed at 1000 °C under nitrogen atmosphere for 30 s [36].

However, to our best knowledge, the effect of the heating rate on the crystallinity and/or on the electrical properties of CeO₂ layers has not been studied. In this present paper, we evaluate the influence of the heating rate of the RTA, with a unique holding temperature, on the morphology and on the crystallinity of CeO₂ layers grown on (111) Si substrate. So we have used different techniques such as Raman Spectroscopy, Photoluminescence, Scanning Electron Microscopy, and tapping mode Atomic Force Microscopy. The impact of the heating rate on the electrical properties of CeO₂ thin film has also been determined by Conductive AFM in order to map the local conductivity of the layer.

2. Experimental

Cerium oxide films were deposited by on-axis radio frequency magnetron sputtering on n-type (111) silicon substrates with an 8–12 Ω cm resistivity. This deposition technique needs some targets. The CeO₂ ceramic targets used were elaborated from cerium oxide powder of 99.95% purity. They were shaped in a mold with a diameter of 35 mm using a uni-axial pressure of 200 MPa. After setting forms, they were sintered in an oven in air using the thermal cycle corresponding to a heating rate of 150 °C/h. The maximum temperature of 1600 °C was held for 2 h.

Silicon substrates were placed in a vacuum system containing a water-cooled rf magnetron sputtering gun operating at 13.56 MHz. In this high vacuum system with a base pressure of 10^{-4} Pa, the plasma was generated by argon gas, which was introduced in the vacuum chamber with a gas flow of 50 sccm. All CeO₂ films were deposited with an rf magnetron power of 60 W, an anode-cathode distance of 3 cm, and a deposition pressure of 10 Pa. The deposition temperature and time were fixed at 600 °C and 40 min, respectively. The thickness of the CeO₂ films is 530 nm. The thickness was measured using a profilometer and the edge of cleaved samples was inspected in a scanning electron microscope. Rapid thermal annealings were performed in a JIPELEC oven at 1000 °C for 30 s under nitrogen atmosphere. The samples suffered three different heating rates of 6. 12 or 25 °C/s, respectively. All these CeO₂ films have been cooled under the same conditions after the RTA and have been characterized by RS, SEM, EDS, PL and tapping mode Atomic Force Microscopy.

The morphology of the CeO_2 films was studied by scanning electron microscopy (Hitachi S3460N and TESCAN-MIRA) and EDS analysis Thermonoran.

Raman spectra were recorded in a backscattering configuration at room temperature using an InVia RENISHAW Raman spectrometer. Helium–cadmium and helium–neon lasers were used as excitation sources with a wavelength of 325 and 633 nm, respectively. The Raman characterization of the different samples was performed with $40 \times$ or $50 \times$ objectives when the wavelength of 325 or 633 nm was selected, respectively. The position (δ) and the Full Width at Half-Maximum (FWHM) of the Raman lines were extracted by fitting with Lorentzian and Gaussian model with an accuracy of 0.2 and 0.3 cm⁻¹, respectively. The measurement dispersion was estimated from statistical analysis and is explained by slight inhomogeneities of the CeO₂ layers. It also takes into account the accuracy of the spectrometer.

Photoluminescence measurements were carried out using an InVia RENISHAW Raman spectrometer with helium– cadmium laser with a wavelength of 325 nm to excite electronic states in the CeO₂ layers.

A Bruker Dimension 3100 AFM with a nanoscope IIIA and a C-AFM module was used for imaging purposes. The Topographic images were obtained in tapping mode, whereas the current images were observed in contact mode. In this work, a conductive probe PtIr coated silicon probe tip with an initial tip radius of 20 nm was chosen. The dc bias was applied to the sample with the tip staying at ground. Measurements were performed at ambient air.

3. Results and discussion

Usually, the impact of post-annealing on the crystallinity of thin film is characterized using X-ray diffraction. However, in a previous paper [28], we have shown that it was difficult to identify the strong XRD peak located near 28.5° , because the Si (111) and CeO₂ (111) peak positions reported in the Joint Committee on Powder Diffraction Standards (JCPDS) files (no. 241402 and no. 340394) are 28.443° and 28.555° , respectively. However, XRD patterns Download English Version:

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