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The origin of forward bias capacitance peak and voltage dependent behaviour of gold/p-type indium phosphide Schottky barrier diode fabricated by photolithography

D. Korucu [a], S. Duman [b,*], A. Turut [c]

[a] Ostim Vocational School, Gazi University, 06500 Ankara, Turkey
[b] Department of Physics, Faculty of Sciences, Ataturk University,25240 Erzurum, Turkey
[c] Department of Physics Engineering, Faculty of Sciences, Istanbul Medeniyet University,34700 Istanbul, Turkey

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ABSTRACT

The admittance measurements which include the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of gold/p-type indium phosphide (Au/p-InP) Schottky barrier diodes (SBDs) were conducted by taking into account the interface states (N_{ss}) and series resistance (R_s) effects in the temperature range of 80–320 K with a steps of 20 K. Experimental results confirm that the N_{ss} and R_s are important parameters which strongly influence the main electrical parameters of SBD. The C–V plots for each temperature exhibit the increasing behaviour in depletion region and then give an anomalous peak such that peak position shifts toward positive bias region with increasing temperature due to the re-structuring and re-ordering of surface charge under the temperature effect and the existence of a series resistance (R_s). In addition, C takes negative values in the inversion region at edge, which is known as negative capacitance (NC) behaviour. The effect of R_s on the C–V plot is found considerably high at low temperatures in the accumulation region. Therefore, both the measured capacitance (C_m) and conductance (G_m/ω) were corrected to obtain the real diode capacitance (C_c) and conductance (G_c/ω). In addition, R_s and N_{ss} values decrease with increasing temperature. Such behaviour of R_s and N_{ss} can be attributed to the trap charges which have sufficient energy to escape from the traps located at gold/p-type indium phosphide (Au/p-InP) interface.

1. Introduction

Metal–semiconductor (MS) and metal–insulator–semiconductor (MIS) type Schottky barrier diodes (SBDs) have a great importance in the electronic applications [1–5]. There are many studies in the literature on SBDs based on III–V semiconductor crystals [5–22]. Among them, InP and its alloys are attractive semiconductor materials due to their wide area applications such as in MS, MIS, metal–insulator–semiconductor field effect transistors (MISFETs) devices, light emitting diodes (LEDs) and solar cells [6–20]. The performance of these devices depends on various parameters such as interface states (N_{ss}) and the formation of barrier height (BH) at M/S interface, series resistance of diode (R_s), the thickness of interfacial layer (native or deposited) and its homogeneity, sample temperature and applied bias voltage [5–12,16–23]. Among them, the N_{ss}, interfacial layer and R_s of the diode are important parameters, which cause the electrical characteristics to be non-ideal. In general, the capacitance–voltage (C–V) and

* Corresponding author. Tel.: +90 442 231 4075; fax: +90 442 236 0948.
E-mail address: sduman@atauni.edu.tr (S. Duman).

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conductance–voltage (G/ω–V) characteristics of SBDs are strongly dependent on temperature.

In recent years, some investigations have reported an anomalous peak in the forward bias C–V plots [24–31]. The origin of such peak has been ascribed to the N_{ss} by Ho et al. [25]. They compared the C–V plots of deposited and annealed silicide–silicon interface. In addition, Werner et al. [26] and Bati et al. [27] have reported that the observed peaks in the forward bias C–V characteristics are due to R_s. In Ref. [26], the origin of the excess capacitance (C_{ex}) can be explained in terms of minority carrier injection. Chattopadhyay and Raychaudhuri [28] showed that C–V characteristics exhibit a peak in the presence of R_s. Also, they have reported theoretically that the peak value of the C–V plots of MIS varies with both N_{ss} and R_s.

In addition, some researchers have reported negative capacitance (NC) in the forward bias C–V plots [11,23,32–39]. The physical mechanism of the NC in different devices such as MS diodes, hetero-junctions, far-infrared detectors, laser diodes, light emitting diodes, photo-detector and some organic semiconductor is obviously different [32–37]. The NC behaviour indicates that the device shows an inductive behaviour. Practically, the NC can be explained by the temperature behaviour and frequency dependent admittance spectroscopy (C–V and G/ω–V) measurements [33]. However, the satisfactory understanding of anomalous peak and NC behaviour in detail has still not been clarified in the literature. It is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states. As can be seen in Ref. [38], the junction capacitance C is a differential effect of charge Q with respect to junction voltage V_j, i.e. $C=dQ/dV_j$. When the forward bias voltage reaches a certain value, the effect of the radiative recombination exceeds that of diffusion. Therefore, the capacitance takes negative value due to positive value of dV_j. On the other hand, at high positive bias voltages, the junction voltage tends to saturate, which means that dV_j takes small values whereas C takes large values. In the ideal case, the magnitude of minority carriers increases exponentially with applied positive bias voltage. Moreover, the more carriers injected, the stronger the recombination velocity. Thus, the value of C reaches to maximum and then decreases rapidly to negative and this decrease in the C corresponds to the increase in the G/ω.

The evaluation of electrical parameters gives detailed information about the nature of diodes. The N_{ss} at M/S interface plays an important role in the determination of the characteristic parameters of the SBDs. Interfaces formed between metals and semiconductors are complex regions whose physical properties depend on the preparation conditions of surface, because in many cases contact metals are deposited onto surfaces covered by unknown contaminants, which may cause the interface states. The surface states can be viewed as electronic states generated by unsaturated dangling bonds of surface atoms [23]. A thin interfacial layer inevitably can be formed during the diode fabrication process. In such case, MS structure is converted to MIS structure. When localized N_{ss} exists at the M/S interface, diode behaviour takes different forms compared to the ideal case. The experimental results obtained by C–V and G/ω–V characteristics are also strongly affected by temperature as discussed in the literature [40–44].

Therefore, in this study, we investigated the temperature and applied bias voltage dependence of forward bias C–V and G/ω–V characteristics to evaluate the effects of N_{ss} and R_s in the temperature range of 80–320 K with bias voltage ranging from -1 to 1 V at 1 MHz. The main goal of this study is the calculation of the characteristic diode parameters such as N_A, Φ_B, R_s, N_{ss} and the evaluation of temperature and voltage dependent characteristics. In addition, to obtain the real C and G/ω, the measured capacitance (C_m) and conductance (G_m/ω) values were corrected as C_c and G_c/ω by eliminating the effect of R_s.

2. Experimental procedures

The Au/p-InP SBD structures were fabricated using p-type single crystal InP wafer with $<100>$ surface orientation, having a thickness of 350 μm, 2 in. diameter and $4–8\times10^{17}$ cm^{-3} carrier concentration (given by the manufacturer). Ohmic contact on the back surface of p-InP was formed by vapour deposition of high purity (99.999%) Al at a low pressure about 1.33×10^{-4} Pa through a thermal evaporation system. After the Al deposition, the sample was annealed at 400 °C for 3 min. The Schottky contacts were formed by the photolithography process onto the front surface through a photo-mask of gold (Au) dots. [45]. The diameter of diode is 200 μm. The capacitance–voltage–temperature (C–V–T) and conductance–voltage–temperature (G/ω–V–T) characteristics of the Au/p-InP SBDs are evaluated in the wide temperature range at 1 MHz by using HP 4192A LF impedance analyser and the test signal of 40 mV peak to peak. The bias voltage is swept from -1 to $+1$ V.

3. Results and discussions

The temperature dependent (C–V) and (G/ω–V) characteristics of Au/p-InP Schottky barrier diodes (SBDs) were measured in the temperature range of 80–320 K with a step of 20 K at 1 MHz and are shown in Figs. 1 and 2, respectively. As can be seen in these figures, both C and G/ω values increase with the increasing temperature in the depletion region. The forward bias C–V plots (Fig. 1) show anomalous peaks due to the existence of R_s, and the magnitude of these peaks decreases and the peaks almost disappear with increasing temperature. These higher values of C and G/ω in the depletion region can be attributed to the excess capacitance (C_{ex}) resulting from N_{ss} in equilibrium with semiconductor and their relaxation time. Obtained results show that the C and G/ω values are strongly dependent on temperature and applied bias voltage [5,11,19–24]

The C–V characteristics show an anomalous peak for each temperature in the forward bias region because of the presence of R_s, N_{ss} and interfacial layer [13,18,24]. The position of the peaks in the C–V plots shifts toward the forward bias region and the magnitude of the peaks increases with the decreasing temperature.

Series resistance (R_s) of the diodes gives rise to some serious error while determining some interfacial properties