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The impact of thermal treatment on gettering efficiency in silicon solar cell

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ABSTRACT

This paper describes a study to understand the impact of heat treatment on the crystal Silicon (c-Si) with developed surface by Aluminum /Porous silicon (Al/PS) and evaluating their influence on the solar cell performance. In fact, the heat treatment of silicon surfaces with PS/Al is an effective means of structural and electrical adjustment and performance improvement of c-Si solar cells. The new process could be accomplished by a two-step annealing in order to benefit from both the high and low temperature processes. The advantages of such a new getter in comparison with traditional getter were demonstrated in various devices. We can estimate that the resistivity using the standard Van Der Pauw, and LBIC measurements have been performed to determine the diffusion length. The resistivity of crystalline silicon decreased when the porous layer was removed at about a depth around 70 μm. As a result, we found amelioration in the *I–V* characteristics and an enhancement of minority carrier lifetime. It has been shown that this simple method leads to improve the charge carrier collection and the electrical properties of c-Si based solar cells.

1. Introduction

In monocrystalline silicon for modern technology application, active areas of microelectronic devices are located in a thin region below the wafer surface. Unlike such a case, the solar cell depended strongly on the bulk of the wafer as being the active device region. Unfortunately, the c-Si solar cells can be generally affected by the unwanted impurities at deep levels in the band gap; which may drastically decrease the minority carrier lifetime, and deteriorate the bulk of length diffusion. Therefore, it is desirable to use the extrinsic gettering techniques at the solar cell fabrication process because solar cells are volume devices. [1–4]. Nevertheless, Al/PS gettering appear to be an efficient and cost effective technique to improve silicon wafers. The Al compound can getters impurities from the silicon substrate by chemical segregation, it has a relatively low diffusivity in Si compared to most other metals. However, a greater solubility for metal impurities than silicon can be provided in the AL/PS layer. [5–11]. It is well admitted that gettering efficiency depends strongly on the type of crystalline silicon and on its history; this suggests that the appropriate gettering can be affected over a wide temperature range [12,13]. However, the gettering effect with heat treatment has been widely discussed in the previous studies due to its benefit for the photovoltaic conversion. Nevertheless, studies about temperature optimization have seldom been reported. In light of these circumstances, efforts have been focused on the development of defect engineering tools in a precise temperature range, such as extended gettering, for further metal impurity concentration reduction that could allow an enhanced gettering effect [14,15]. However, it is necessary to consider two steps annealing in order to take into account the effect of each step on the metal impurity concentrations within the Si material for these purposes. The crucial first step at high temperature included the solar

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cell fabrication process, thereby; precipitate dissolution impurities can be expected. Then, the impurities cooled down at low-temperature where they received a new gettering. This technique of two-step annealing has been used to facilitate an excellent control profile without precipitation and surface segregation effects.

In this study, we demonstrated that it is possible to enhance silicon wafer purification by two-step annealing. Further, we reported electrical results in order to evaluate the effect of two-step annealing in the same silicon.

2. Experimental procedure

The used substrates are Czochralski (Cz) low-cost, oriented (100), and p-type boron doped silicon, with a resistivity ranging from 1 to 2 Ω cm and a thickness of about 200 μm. The wafers were dipped in an acid mixture solution (HF: 16%, HNO_3: 64%, CH_3COOH: 20%) for a few seconds, then they were rinsed in deionized water. A thin porous layer was formed on both sides of the sample by stain-etching of the wafers in an $HF/HNO_3/H_2O$ solution with 1:3:5 volume compositions. Then, a thick aluminum layer was evaporated onto both sides of samples.

In order to optimize the range temperature and improve the electrical quality, the Cz wafers were individually annealed in either one or two steps. This experimental is organized as follows:

First treatment: samples (C1) were thermally treated at 750 °C for 30 min in N_2 ambient.

Second treatment: samples (C2) were thermally treated at1050 °C for 30 min in N_2 ambient.

Third treatment: samples (C3) were thermally treated at 1050 °C for 25 min and cooled down to 750°C where the wafers received a gettering anneal in N_2 ambient for 30 min.

C0 is an untreated sample taken as a reference for comparison.

After the heat treatment and in order to remove the PS/Al layer, we immersed these samples successively in an HF and NaOH (1 N) solutions. Then, the wafers to be studied were separated into three sets. The first set was used for developing an $Al/SiO_2/Si–SiO_2/Si$ structure. The MIS ($Al/SiO_2/Si$) structure was deployed for the LBIC method that proved to be much more sensitive to fine detail than channeling measurements. At the second step, we carried out resistivity measurements using the standard Van der Pauw. The third set to be used with the c-Si solar cells was achieved by performing phosphorus diffusion in a rapid thermal infrared tubular furnace at 925 °C for 30 min. The back aluminum (Ag/Al) and the front contact (Ag) were made by screen printed and fired at 850 and 620 °C respectively. The minority carrier lifetime was measured by a Sinton WTC-120 set-up with the intention. The electrical characterization (*I–V*) was measured by a source meter keithley 2400. The data were analyzed by software origin.

3. Results and discussion

3.1. Minority carrier lifetime

Table 1 illustrates the variation of the effective minority carrier lifetime τ_{eff} for each treatment after being immersed in 0.1 M concentrated I–E solution [16,17]. The effective lifetime τ_{eff} is the net result of summing up all the recombination losses that occur within the different regions constitutive of a given silicon sample.

Table 1
Variation of minority carrier lifetime values from top surface of solar cells with the treatment conditions.

Samples	C0	C1	C2	C3
τ_{eff} (μs)	4.88 ± 0.9	21.68 ± 1.15	14.7 ± 1.07	24.87 ± 1.26

All lifetime measurements were taken through the photoconductance lifetime tester (WTC 120 Sinton) technique. The latter is based on the measurement of the relative change of Δn with time. A simple flash lamp is used to produce a slowly varying illumination and a resulting time dependence of the excess photoconductance of the sample. The analysis of data determined the effective minority carrier lifetime. All reported lifetimes were measured at an injection level of $1 \times 10^{15}\,cm^{-3}$. According to this formula (1)

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{\omega} \quad (1)$$

where τ_{bulk}: the bulk lifetimes; S_{eff}: the surface recombination velocities and ω is the thickness of the c-Si substrate.

The measured effective lifetime is equivalent to the actual lifetime bulk when the surfaces are well passivated. Nevertheless, the demands on surface passivation can be relaxed when determining the relatively bulk lifetimes. This suggests that the differences between surface recombination rates and samples are not substantial. In this case $(1/\tau_{eff}) \cong (1/\tau_{bulk})$.

The effective lifetime of bare c-Si wafer untreated was measured as 1.2 μs, which increased to 4.88 μs after passivation although some native dangling bonds near the surface are saturated.

The effective lifetime is significantly different for the samples and more significative depending on the process history of the sample.

As mentioned above, a significant change of the τ_{eff} after annealing at 750 °C was observed, which determined a decrease of impurities diffused into the gettering zone. The corresponding increase in lifetime is further enhanced with the 1050–750 °C combination. We observed lifetime degradation in the wafer treated at extremely high temperature annealed at 1050 °C

Nonetheless, we can make several tentative conclusions from the lifetime results which are briefly discussed below.

3.2. Diffusion length

To investigate whether an effect to the sample interior could be observed. A second, equally important aspect of the lifetime is that it is directly related to the diffusion length. The lifetime is primarily used in integrated circuit engineering whereas the diffusion length measurement is more commonly specified for photovoltaic.