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Thin layer oxide in the drift region of Laterally double-diffused metal oxide semiconductor on silicon-on-insulator: A novel device structure enabling reliable high-temperature power transistors

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ABSTRACT

In this paper a new lateral double diffused metal oxide semiconductor (LDMOS) transistor on silicon-on-insulator (SOI) technology is reported. In the proposed structure a trench oxide in the drift region is reformed to reduce surface temperature. In the LDMOS devices one way for achieving high breakdown voltage is incorporating the trench oxide in the drift region. But, this strategy causes high lattice temperature in the device. So, the middle of the trench oxide in the drift region is etched and filled with the silicon to have higher thermal conductivity material and reduce the lattice temperature in the drift region. The simulation with two-dimensional ATLAS simulator shows that the novel thin trench oxide in the n-drift region of LDMOS transistor (TT-LDMOS) have lower maximum lattice temperature with an acceptable breakdown voltage in respect to the conventional LDMOS (C-LDMOS) structure with the trench oxide in the drift region. So, TT-LDMOS can be a reliable device for power transistors.

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1. Introduction

In the recent years, lateral double diffused metal oxide semiconductor (LDMOS) transistors have been extended to the SOI technology to sustain high breakdown voltage [1–3]. Also, in the SOI technology many advantages such as superior isolation, low parasitic capacitances, and high integration density characteristics have been reported [4–9]. In another vision, a trench oxide in the drift region of the LDMOS transistors reaches high breakdown voltage in comparison to the conventional LDMOSs [10,11]. But, incorporating the trench oxide in the SOI-LDMOS structures raises maximum lattice temperature in the device. The trench oxide has lower thermal conductivity and acts as a barrier for the heat dissipation at the surface. Thus, when high drain voltage is applied to the power devices, the temperature rises in the drift region than the conventional LDMOS without the trench oxide due to the heat generation. In the previous efforts, many structures had been proposed to reduce the thermal problems of the trench oxide [12–14]. These techniques reduce maximum lattice temperature in the device, but degrade the blocking voltage.

In this paper a new structure of the trench oxide LDMOS device is proposed to reduce maximum lattice temperature of the device with an acceptable breakdown voltage.

The goal of this work is using the thin layers of silicon oxide in the drift region. In other words, the middle of trench oxide in the drift region is etched and the silicon is replaced in which thin layers of oxide remain. The simulation with

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two dimensional ATLAS simulator shows that the novel thin trench oxide in the n-drift region of LDMOS transistor (TT-LDMOS) reduces the maximum lattice temperature of the device, efficiently. This behavior is due to the higher conductivity of silicon than the silicon oxide [15]. Also, incorporating thin layers of the oxide causes high breakdown voltage [12]. So, the TT-LDMOS structure is more reliable than the conventional structure for high temperature applications of power devices.

2. Device structure

The schematic cross-section of the TT-LDMOS on SOI technology is shown in Fig. 1(a), featuring alternating regions with the thin trench oxide that is located in the drift region. As the figure shows, the length and depth of the thin trench oxide are labeled as L_{ox} and D_{ox}, respectively. Also, Fig. 1(b) shows the conventional LDMOS (C-LDMOS) structure with the trench oxide in the drift region.

Numerical simulations were performed by solving Poisson, drift/diffusion equations and heat equation plus SHR (Shockley–Hall–Read) and Auger generation/recombination and impact ionization processes. Carrier velocity saturation, carrier–carrier scattering at high doping and dependence of mobility on temperature and transverse electric field [15] are accounted for. Also, in the simulation, the boundary condition of the heat flow is fixed at 300 K at the bottom interface of the silicon substrate. However thermo contact is used for considering temperature variation and self-heating effect. The self-heating effect can be described as the deviation between the non-isothermal and isothermal behaviors in the simulations. It is important to note that the Newton method is used for solving the equations. Also, the TT-LDMOS and C-LDMOS parameters that are used in ATLAS simulations are shown in Table 1.

The fabrication processes of the TT-LDMOS are proposed in Fig. 2. The process starts with the conventional LDMOS transistor as it is shown in step (1). In step (2) the trench oxide should be created in the drift region. This SiO_2 region can be created with the separation by implementation of the oxygen (SIMOX) method [16]. The next process (4) is etching the specific area in the trench oxide to create thin layers of oxide. Then, the empty region should be filled with the silicon material and the ion phosphors should be diffused in the silicon layer to have the same doping concentration as

Table 1
Typical parameters for TT-LDMOS used in ATLAS simulations.

Device parameters	Value (TT-LDMOS)	Value (C-LDMOS)
Gate length (L_G)	5 μm	5 μm
Channel length	3 μm	3 μm
Drift region length	10 μm	10 μm
Silicon thickness	0.6 μm	0.6 μm
Gate oxide thickness (t_{ox})	50 nm	50 nm
Trench oxide length (L_{ox})	6 μm	6 μm
Trench oxide depth (D_{ox})	0.2 μm	0.4 μm
Buried oxide thickness	0.3 μm	0.3 μm
Drift region doping concentration	5×10^{15} cm^{-3}	5×10^{15} cm^{-3}
Channel doping concentration	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
Source/drain doping concentration	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Substrate doping concentration	5×10^{13} cm^{-3}	5×10^{13} cm^{-3}

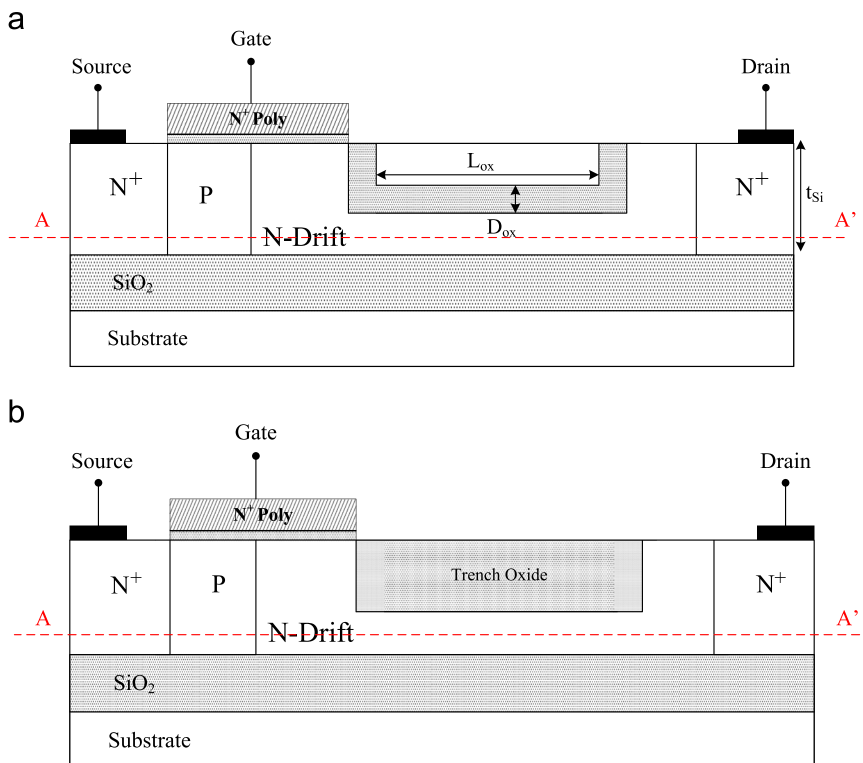

Fig. 1. Schematic cross section of (a) TT-LDMOS structure, (b) C-LDMOS transistor.

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