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# Numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor

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ABSTRACT

We report on a numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor (GaAs FET) using proprietary simulation software. The substrate is assumed to contain shallow acceptors compensated by deep levels. The ratio between the densities of deep and shallow levels is considered to be one hundred, which is a typical value for semi-insulating substrates. Although several traps may be present in the substrate but only the most commonly observed ones are considered, namely hole traps related to Cu and Cr, and the familiar native electron trap EL2. The current–voltage characteristics of the GaAs FET are calculated in the absence as well as in the presence of the above mentioned traps. It was found that the hole traps are affected by the gate voltage while the electron trap is not. This effect on the response of hole traps is explained by the fact that the quasi-hole Fermi level in the substrate is dependent on the gate voltage. However, the electron quasi-Fermi level in the substrate is insensitive to the gate voltage and therefore electron traps are not perturbed.


## 1. Introduction

Gallium arsenide (GaAs) based devices such as field effect transistors (FETs), high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are used in many applications in the electronics industry. GaAs FETs and HEMTs are the main components in monolithic microwave integrated circuits (MMICs), which are widely used in high speed and high frequency applications. Discrete devices as well as integrated circuits are fabricated on semi-insulating (SI) substrates, where the residual shallow donors and/or acceptors are compensated by deep-level traps. The semi-insulating property enables good isolation between adjacent devices in MMICs, and hence minimizes parasitic capacitances. However, deep-level traps in the SI substrate are believed to cause many undesirable effects in GaAs devices and circuits including drain and gate lag [1–3], frequency dispersion of conductance and transconductance [4–7], low frequency oscillation [8] and backgating [9–13]. Great efforts have been made to suppress or at least reduce substrate trapping effects for example by inserting a buried p-layer between the conducting channel and the SI-substrate [14]. However, these traps are still of great concerns for GaAs and other III–V based devices and circuits [15–17].

Unlike in simple structures, such as p–n and Schottky junctions, deep traps need not only to be identified but also accurately located in the more complicated geometry of a GaAs FET. Since its introduction in 1974 by Lang [18],

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Deep Level Transient Spectroscopy (DLTS) has become the most common method to characterise deep-level traps. A common observation in DLTS spectra of GaAs FETs is the presence of electron-like traps (deep donors) such as the nativeEL2 level and a large number of hole-like traps (deep acceptors) with large concentrations [19]. The possible location of traps in GaAs FETs can be (i) at the surface of the un-gated regions of the channel, (ii) in the channel, (iii) in the SI substrate or (vi) at the channel/SI substrate interface. However, hole-like traps are not likely to be active in the n-type channel since the hole quasi-Fermi level cannot cross their energy levels [20]. In addition, hole-like traps are not expected to be located near the channel/SI substrate interface or in the SI substrate due to the fact that there is a response to a voltage applied to the gate. Zylberstejn et al. [20] suggested that the ability of a gate voltage to disturb the population of SI-substrate related traps is due to the relative displacement of the quasi-Fermi levels in the Schottky and the channel/substrate interface regions. However, as far as the authors know, there was no attempt to elucidate this phenomenon by any means except for the analytical modelling of the drain current transient caused by a substrate trap following a pulse on the gate [21]. In Ref. [20] it was assumed that a space charge exists at the channel/SI substrate interface, and the process of trapping/de-trapping charges widens or narrows it. Previously we have used a numerical simulation to correlate the existence or absence of a backgating threshold voltage to the type of deep levels in SI substrates (acceptors or donors) [22]. In this work we use the ATLAS module of the SILVACO TCAD software [23] to investigate the effect of the different traps present in the substrate on the current–voltage characteristics of the transistor. The quasi-Fermi levels are used to explain the ability of some SI substrate traps to respond to the gate voltage. Numerical simulation has the unique feature that internal parameters, such as the potential profile, the trap occupation and the quasi-Fermi levels, can be evaluated. This, obviously, cannot be achieved by experimental work or analytical modelling.

## 2. Sample structure

The channel of the GaAs FET used in this work is n-type with a density of $5 \times 10^{16}$ cm$^{-3}$ shallow levels. The gate is a metal which induces a Schottky type potential barrier, assumed to be around 0.7 V, resulting from the difference between the metal and semiconductor work functions [24]. The substrate is assumed to contain shallow levels compensated by deep levels with the density of the latter exceeding that of shallow levels [25]. In this work we have considered a ratio of 100 between the densities of deep and shallow levels which is an acceptable value for typical semi-insulating substrates. Although there may exist several traps in the SI substrate we only took into account the most commonly observed ones: namely HL1, HL4 and EL2 [26,27]. HL1 and HL4 are hole-like traps and are related to Cu and Cr, respectively, while EL2 is the familiar electron trap. EL2 is a native defect which is almost present in any GaAs sample and may be its alloys like AlGaAs. More details can be found in Ref. [25]. The channel and substrate thicknesses are 0.2 and 10 μm, respectively. A two dimensional cross section along the channel of the GaAs MESFET structure used in this work is shown in Fig. 1.

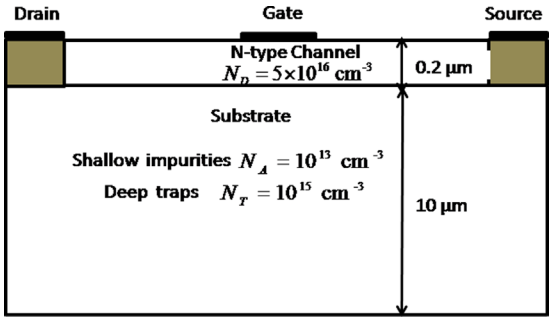


**Fig. 1.** A two dimensional view of the GaAs MESFET structure simulated in this work. The channel is 0.2 μm thick and doped with $N_D = 5\times 10^{16}$ donors/cm$^{-3}$, the substrate is 10 μm thick where shallow residual impurities $N_A = 10^{13}$ acceptors/cm$^{-3}$ are compensated by $N_T = 10^{15}$ traps/cm$^{-3}$.

## 3. Numerical simulation

In order to characterise semiconductor devices and correlate the observed effects to each other, extensive experimental work has to be carried out. In some cases, analytical or qualitative modelling has to be used to relate these experimentally observed effects. The experimental characterisation is time consuming and can be very expensive. The analytical modelling includes several simplifications. Numerical simulation is an alternative and a powerful tool. Many parameters can be varied to model the observed phenomenon. In this present study the variables are the defects and the phenomenon is the current–voltage characteristics as well as the quasi-Fermi levels. Numerical simulation can also offer a physical explanation of the observed phenomenon since the internal parameters can be calculated including the electrical field and the free carrier densities.

The electrical characteristics of the devices are calculated using ATLAS of SILVACO. It is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation. The simulator is based on a mathematical model valid for any semiconductor device. This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the carrier continuity equations and the transport equations.

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models. The simplest model of charge transport that is useful is the drift–diffusion model [24]. This model is adequate for nearly all devices that can be technologically fabricated. This model is based on the two first equations cited above.