Materials Science in Semiconductor Processing 24 (2014) 278–281

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Theoretical determination of the impact of channel morphology and quantum size effects on the surface potential of nanocrystalline silicon thin film transistors

Rachid Fates [a,b,*], Hachemi Bouridah [a,b], Riad Remmouche [a,b]

[a] LEM Laboratory, Jijel University, B.P. 98, Ouled Aissa, Jijel 18000, Algeria
[b] Department of Electronic, Jijel University, B.P. 98, Ouled Aissa, Jijel 18000, Algeria

ARTICLE INFO

Available online 22 April 2014

Keywords:
Nanocrystalline silicon
Nanocrystallites size
Granular morphology
Surface potential

ABSTRACT

In this work, we propose an analytical model allowing the calculation of nanocrystalline silicon thin film transistors surface potential by considering a granular morphology of silicon nanocrystallites forming the channel. Results show that, according to the quantum effects on dielectric constant and band gap, the surface potential values are strongly related to the silicon crystallites structure in terms of size and geometry. The comparison of our results with existing research data shows a good agreement between the surface potential shapes and an interesting difference in the surface potential variations related to the morphology specificity considered in our theoretical approach.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

The production of polycrystalline (either with micro or nano dimensions) silicon (poly-Si) thin films have been under development since a few years ago. The research interest in this field envisages the devices improvement for micro and optoelectronic applications. The active-matrix liquid–crystal displays (AMLCDs) commercial success has stimulated considerable research on thin-film transistors (TFTs), which are function of the pixel switches in AMLCDs [1–3].

Nanocrystalline silicon (nc-Si) is a compromise solution between amorphous silicon (a-Si) and poly-Si. It is a good alternative to a-Si since it offers higher carriers mobility, and its application in TFTs is recent. The nanostructural properties of nc-Si films are important issue for these device applications. The consideration of nc-Si structure for circuit design and simulation is thus vital to a rational description of the electrical and the electronic behavior of the device [4–6]. Several authors have made significant studies concerning the different voltage relationships for poly-Si TFTs [7,8]. However, few researches have focused on the study of the nc-Si TFTs electrical characteristics. L.F. Mao [9] has developed a surface potential model for nc-Si TFT. A mono-energetic trap state was adopted in Mao's model without any consideration of the nanocrystallites geometry forming the channel.

In the present study, we propose a new theoretical approach allowing the surface potential analytical calculation by taking into account the channel nanometer crystalline structure in terms of crystallites geometry and size. A U-shaped density of states is used in our model.

2. Surface potential model

We present in Fig. 1 a TFT channel three dimensional description with a granular morphology characterized by nanometric crystallites size. We consider the silicon nanocrystallites as a set of grains with nanometer sizes and

* Corresponding author at: Department of Electronic, Jijel University, B.P. 98, Ouled Aissa, Jijel 18000, Algeria.
E-mail address: rachid.fates@yahoo.fr (R. Fates).

http://dx.doi.org/10.1016/j.mssp.2014.03.025
1369-8001/© 2014 Elsevier Ltd. All rights reserved.

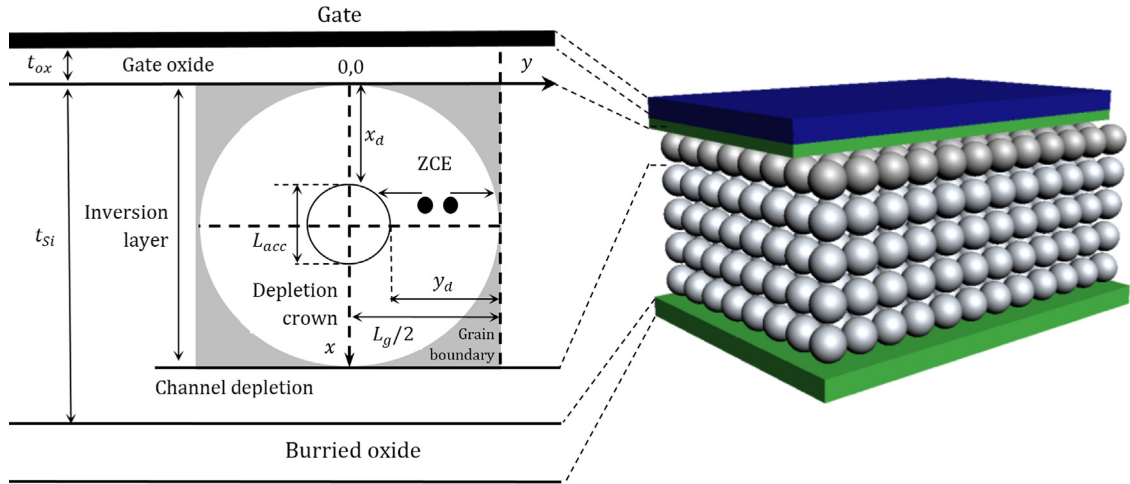

Fig. 1. Right, nc-Si TFT granular channel morphology. Left, channel surface grain cross section at strong inversion.

spherical geometry, separated from each others by an amorphous region (grain boundary).

We assume that in the inversion layer (represented by a grains cluster at the channel/gate-oxide interface), the adjacent electrons induced by a positive gate voltage value are trapped into the grain boundary, which causes the depletion region formation within the grains. Then, by applying Gauss's theorem in x and y directions [7,10], the following equation can be derived

$$\varepsilon_{si}\int_0^{L_{acc}/2}\int_0^{L_{acc}/2}\left[\frac{\partial\psi(x,y)}{\partial x}+\frac{\partial\psi(x,y)}{\partial y}\right]dxdy + C_{ox}\int_0^{y}\int_0^{x}[V_{gs}-V_{fb}-\psi(x,0)-\psi(0,y)]dxdy = qN_aL_{acc}xy \tag{1}$$

where L_{acc} is the grain accumulation charge depth, $\psi(x,y)$ is the electrostatic potential, V_{gs} is the gate-source voltage, V_{fb} the flatband voltage, N_a is the p-type substrate doping concentration, C_{ox} is the gate oxide capacitance per unit area $(\varepsilon_{ox}/t_{ox})$, t_{ox} is the gate oxide thickness, and ε_{ox} and ε_{si} are the permittivity of silicon-oxide and silicon, respectively. We assume that the electrostatic potential has a circular distribution with x-axis and y-axis. Therefore

$$\psi(x,y)=[\psi(x,0)+\psi(0,y)]\left[\left(\frac{x}{L_{acc}/2}\right)^2+\left(\frac{y}{L_{acc}/2}\right)^2-1\right] \tag{2}$$

substituting Eq. (2) into Eq. (1), differentiating both sides with respect to x and y, and after some algebraic manipulations, Eq. (1) becomes

$$\frac{\partial^2\psi(x,0)}{\partial x^2}+\frac{\partial^2\psi(0,y)}{\partial y^2}=\left(\frac{2C_{ox}}{\varepsilon_{si}L_{acc}}\right)[\psi(x,0)+\psi(0,y)] - \left(\frac{2C_{ox}}{\varepsilon_{si}L_{acc}}\right)\times\left(V_{gs}-V_{fb}-\frac{qN_aL_{acc}}{C_{ox}}\right) \tag{3}$$

where L_{acc} can be approximated as follows [7]

$$L_{acc}=\sqrt{\frac{4\varepsilon_{si}\psi_{S0}}{qN_a}} \tag{4}$$

where ψ_{S0} is the potential at the crystallite contact with gate-oxide, given by

$$\psi_{S0}=\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)+\frac{E_i-E_v-\chi_0}{q} \tag{5}$$

where E_i is the intrinsic level, E_v is the valence level, n_i is the intrinsic concentration and χ_0 is determined from the following equation [7]

$$[E_g-\chi_0-q\phi_b]N_D^D+N_D^TE_D^T\exp\left[-\frac{\chi_0+q\phi_b}{E_D^T}\right]=N_aL_g \tag{6}$$

where E_g is the band gap, N_D^D is the deep donors states density, E_D^T is the tail donors states level, N_D^T is the tail donors states density, L_g represents the grain diameter and ϕ_b is the barrier height in the substrate given by

$$\phi_b=\frac{qN_a}{2\varepsilon_{si}}\left(\frac{L_g}{2}\right)^2 \tag{7}$$

under the following boundaries conditions

$$\psi(0,0)=\psi_{S0}\ and\ \left.\frac{\partial\psi(0,y)}{\partial y}\right|_{y=0}=\left.\frac{\partial\psi(x,0)}{\partial x}\right|_{x=0}=0$$

the solution of Eq. (3) represents the electrostatic potential at the grain boundary. It can be expressed as

$$\psi(x,y)=2\left(V_{gs}-V_{fb}-\frac{qN_aL_{acc}}{C_{ox}}\right)+\left(\frac{\psi_{S0}}{2}-V_{gs}+V_{fb}+\frac{qN_aL_{acc}}{C_{ox}}\right)\times\left\{\cosh\left[\left(\frac{2C_{ox}}{\varepsilon_{si}L_{acc}}\right)^{1/2}x\right]+\cosh\left[\left(\frac{2C_{ox}}{\varepsilon_{si}L_{acc}}\right)^{1/2}y\right]\right\} \tag{8}$$

We suppose that at the onset of strong inversion and under the charge trapping at the grain boundary, the depletion along x-axis, x_d, should be matched with the depletion along y-axis, y_d. Then, we obtain a crown depletion form around the center of each crystallite juxtaposed with the channel/gate-oxide interface as illustrated in Fig. 1. As the gate voltage increases further, in spite of the trapping effect at grain boundary, the inversion region starts to occur at a location far from grain boundary, in other terms, at the center of each grain [11]. Thus, Eq. (8)

Download English Version:

https://daneshyari.com/en/article/729378

Download Persian Version:

https://daneshyari.com/article/729378

Daneshyari.com