Materials Science in Semiconductor Processing 13 (2010) 344–348

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

TCAD modeling of NPN-SI-BJT electrical performance improvement through SiGe extrinsic stress layer

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ARTICLE INFO

Available online 30 March 2011

Keywords:
Bipolar
Mobility
Si BJT
SiGe HBT
Strain
Stress
Transistor

ABSTRACT

The impact of introducing a SiGe stress layer formed over the extrinsic base and adjacent to the intrinsic base of NPN-Si-BJT device on the electrical properties and frequency response has been studied using TCAD modeling. Approximately 42% improvement in f_t and 13% improvement in f_{max} have been achieved for the strained NPN-Si-BJT device in comparison with an equivalent standard conventional BJT device. In addition to that, an enhancement of the collector current by almost three times has been achieved. The same approach has been applied for NPN-SiGe-HBT device to clarify the impact of the extrinsic SiGe stress on the device's performance using TCAD modeling. Simulation results have shown that applying the SiGe stress layer on the base region of the HBT device is less efficient in comparison with the BJT device, as the SiGe base is already stressed due to the existence of Ge at the base. Approximately 5% improvement in f_{max} and 3% improvement in f_t have been achieved for the strained HBT device in comparison with an equivalent standard conventional HBT device.

1. Introduction

With the continuing reduction in dimensions of electronic devices , it becomes imperative to develop new Si bipolar architectures suitable for high frequency and power applications. Therefore, various techniques and efforts have been proposed to improve the performance of bipolar devices: introduction of germanium into the base [1], introduction of carbon to improve 1D doping profile [2], and reduction of the emitter width [3]. An additional way to improve the device performance is to enhance the carrier transport by changing the material properties using strain engineering technology [4–7]. Mobility of charge carriers in bipolar devices can be improved by creating mechanical tensile strain in the device in the direction of electron flow to improve electron's mobility, and by creating mechanical compressive strain in the direction of hole flow to improve hole's mobility [8]. The compressive and tensile strains are created by introducing an extrinsic stress layer with different lattice constant in the device [9]. In our case, the extrinsic stress layer is a SiGe layer with a specific Ge content implemented in the device to achieve the desired strain effect.

2. Process Simulation

Process simulations are performed using Sentaurus TCAD software tools to build the device structure and to calculate the associated mechanical stress using anisotropic elasticity model [10]. The major fabrication process steps used in this work are similar to the ones reported by Van Huylenbroeck et al. [11]. The complete proposed strained NPN-Si-BJT device structure is shown in Fig. 1. For simulation efficiency and saving simulation resources,

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doi:10.1016/j.mssp.2011.03.002

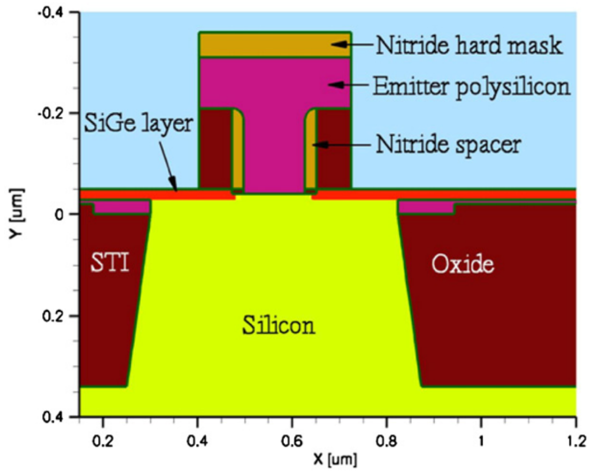

Fig. 1. Complete proposed strained NPN-Si-BJT device structure with SiGe extrinsic stress layer.

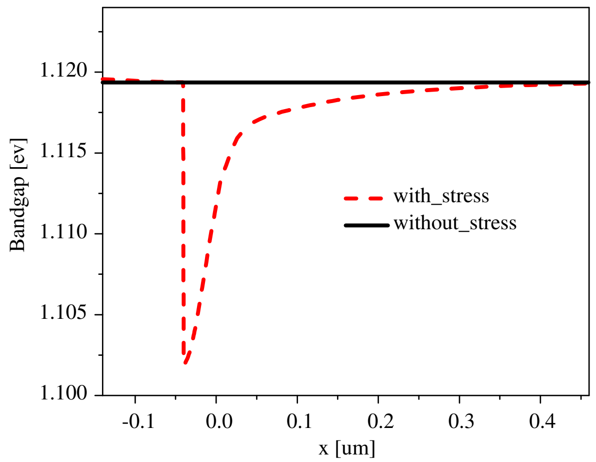

Fig. 3. Impact of stress on the device bandgap energy (Ge=25%, W_E=130 nm).

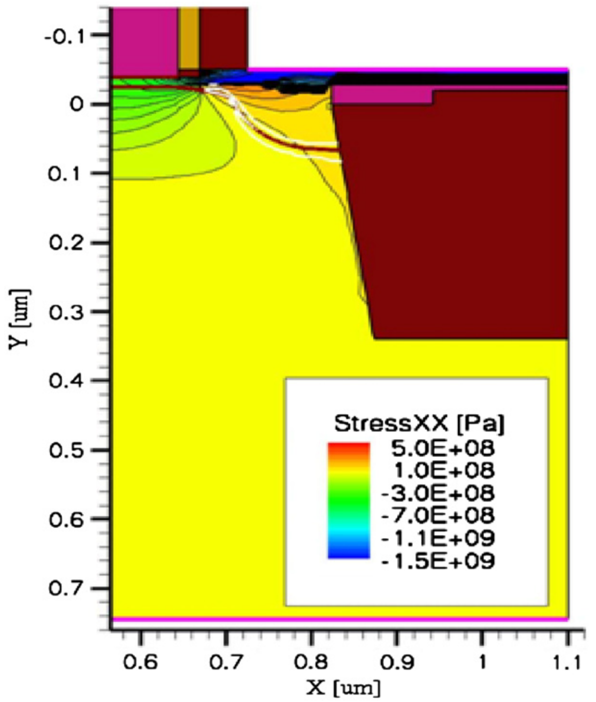

Fig. 2. Cross section of one half of the device; isocontour stress lines representing the stress (S_{xx}) induced in the *x*-direction of the structure.

only half of the device is used for further device simulations. The simulated effect of interposing the extrinsic stress layer at the device is shown in Fig. 2; the isocontour lines represent the stress values generated in the *x*-direction (S_{xx}) due to the existence of the extrinsic SiGe stress layer.

3. Impact of strain

Mechanical stress on semiconductors induces a change in the band structure and this in turn affects the carrier mobility. This effect can be explained by the deformation potential theory [12]. Strain changes the number of carrier sub-valleys and eventually a change in the actual bandgap in the material [13]. The carrier redistribution that takes place between the various sub-valleys causes the change in mobility. The mobility enhancement is attributed to the increase in the occupancy of the conduction band valleys [14]. The impact of introducing a SiGe strain layer in the BJT device's architecture on the device's bandgap energy is shown in Fig. 3. As shown in the figure, introducing SiGe strain layer formed over the extrinsic base and adjacent to the intrinsic base of NPN-Si-BJT device causes a reduction in the device's bandgap energy, which will result in an improvement in the electrons injection efficiency from emitter to collector and an enhancement of the device's electrical performance.

4. Electrical Characteristics

TCAD software tools have been used to perform the two-dimensional device simulations using hydrodynamic transport model, where the carrier temperature equation for the dominant carriers is solved together with the electrostatic Poisson equation and the carrier continuity equations [15]. The carrier mobilities have been calculated using Philips unified mobility model, the high field saturation was calculated through the Canali model using the carrier temperatures as the driving force. The carrier generation–recombination models used are the Shockley–Read–Hall recombination model and Auger recombination model. As well, the doping-induced bandgap narrowing model has been employed. Furthermore, the stress-induced mobility enhancement has been calculated using the Piezoresistivity model. The graded Ge profile and the doping profiles at the emitter, the base, and the collector regions have been taken from the IMEC Microelectronics bipolar device profile [16]. The parameter files and physical models used have been calibrated using Monte Carlo simulations [17].