Measurement 69 (2015) 31–41

Contents lists available at ScienceDirect

Measurement

journal homepage: www.elsevier.com/locate/measurement

Implementation of a field programmable gate array-based lock-in amplifier

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ARTICLE INFO

Article history:
Received 28 May 2014
Accepted 13 February 2015
Available online 18 March 2015

Keywords:
Lock-in amplifier
Field programmable gate array
Photoacoustic effect

ABSTRACT

A Lock-In Amplifier (LIA), or phase sensitive detector, is an instrument capable of providing high frequency selectivity allowing the user to distinguish a signal of interest from background noise, and has become an important component in the instrumentation for the study of many different physical phenomena. In this work a LIA is implemented using digital signal processing techniques on a field programmable gate array, or FPGA, and is compared against a commercial counterpart with the objective of showing that homebrewed instruments can produce reliable and trustworthy results. For this comparison experimental tests have been performed which are based on the photoacoustic effect, given that LIAs are cornerstones of many techniques based in this and other related effects.

1. Introduction

Noise is everywhere; incoherent signals which contain no information of interest. Electronics and digital technology are a big part of our modern day world and electronic noise can be particularly troublesome, especially when a small coherent signal must be detected in an ocean of noise. Recovering such signals is an extremely important task in modern laboratories since many of the phenomena studied generate only small changes in the transducers used to measure them.

A technique that can overcome the problems introduced by noisy signals is Phase Sensitive Detection, also known as Lock-in Amplification. A Lock-in Amplifier (LIA) is a device capable of reconstructing a signal with a known carrier wave from an extremely noisy background. The Amplifier, through a mixer, turns the quadrature and in-phase components of the signal into non time varying information. Extracting a non-time varying signal can be done far more efficiently than extracting the original signal, giving this technique an edge over traditional filtering. A LIA's operating principle has been described elsewhere (see for example Ref. [1,2], and references herein). In a few words, from the input signal $S(t)$, and knowing the reference frequency, the function of a LIA is to recover the in-phase, $I = A\cos(\phi)$, and quadrature, $Q = A\sin(\phi)$, components, from which the amplitude and phase can be determined as $A = (I^2 + Q^2)^{1/2}$ and $\phi = \arctan(Q/I)$ respectively.

A LIA may be implemented using analog or digital techniques. The digital revolution has brought implementation costs down and using Digital Signal Processing (DSP) techniques one may construct a Digital LIA (DLIA) with modest resources. Implementing a LIA using digital technologies can have several advantages over analog constructions. For starters, the ever falling price of digital systems (DS) has made the cost-benefit ratio extremely attractive. Also the computing power of DS has increased to the point where DSP techniques surpass their analog counterparts in most cases due to their inherent immunity to noise, the exception being very high frequency applications and even in that area the line is beginning to fade.

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http://dx.doi.org/10.1016/j.measurement.2015.02.037
0263-2241/

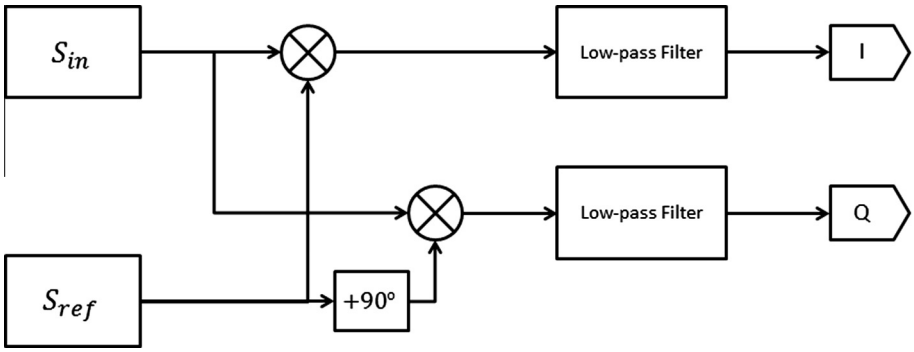

Fig. 1. Basic LIA block diagram.

Implementing a DLIA makes sense in the modern day world. Many of the commercial models available are indeed digital rather than analog. A major difference when pursuing a digital implementation is that the Nyquist–Shannon sampling theorem must be met in order to not introduce aliasing errors into the system [3]. Different types of digital devices would be capable of implementing a DLIA. Digital signal processors, for example, are microprocessors with an architecture that has been thought around the needs of DSP. However on a Field Programmable Gate Array (FPGA) the user is actually designing the hardware, instead of just the algorithms as would be the case on microprocessors. In essence, bringing a DLIA to life through a FPGA would not just describe the different mathematical operations needed, but would also to some level describe the device as physical hardware. [4] On a FPGA several parallel running components may be implemented without much hassle. This can be translated into an increased efficiency and ease of implementation for many DSP techniques. Thus, it is the subject of this work to implement a DLIA on a Field Programmable Gate Array (FPGA) and compare it against a commercial model.

2. Architecture and implementation

A simplified block diagram of a LIA is shown in Fig. 1. The input signal S_{in} is polluted by noise. In a digital implementation the signal must be filtered to comply with the Nyquist sampling criteria (said filter is not shown in the figure) [5]. A reference signal S_{ref}, of which we have full control of both phase (ϕ) and frequency (f), is fed into the system. S_{ref} must drive or sync the system generating S_{in}. S_{ref} is then phase-shifted by 90° (quadrature) generating two reference orthogonal waves at f, which are then multiplied with signal S_{in}, a process sometimes known as mixing [6]. Mixing two sinusoidal functions will generate a non-oscillatory component dependent on the relative phase of said functions and their amplitude. This non-oscillatory signal can be extracted by low-pass filtering the signal. This filtering process is applied to the result of both multiplications, with the in-phase component being called "I" and the quadrature component "Q". I & Q can now be used to reconstruct the original signal.

The Spartan 3E-1600 Development Board produced by Digilent Inc. has been chosen for this project, its characteristics can be found elsewhere [7]. It is a self-contained development platform which features a Spartan 3E FPGA from Xilinx, the chip features the equivalent of 1600K gates and is capable of realizing complex digital systems. The board contains most of what is needed for the implementation of a DLIA, including a 14-bit analog to digital converter or ADC (Linear Technologies LTC1407A-1), a programmable preamplifier with a maximum amplification of 100 (Linear Technologies LTC6912-1), several communication interfaces and multiple input and output pins as well as integrated clock oscillators. The board also provides many more features, which although not essential to the implementation of the DLIA invite for further development and experimentation.

The method of choice for configuring the Spartan 3E is through a Hardware Description Language (HDL). For this project very high speed integrated circuit Hardware Description Language (VHDL) has been chosen over verilog, which are the two most common HDL.

The DLIA design and code is in itself portable and is not limited to running on a Spartan 3E, other models and manufacturers may be used with little modifications which would be related to any variations in the hardware peripherals being used (namely the ADC and communication interface) and the pin-out of the chip being used.

The construction of a DLIA may now be split into the categories shown in Fig. 2. The DLIA will be controlled by a series of registries to which an external device (a PC for most cases) will be able to perform read and write operations. Some of these registries are interpreted as instructions by the DLIA, while others are used to report the results.

2.1. Analog to digital conversion

2.1.1. Analog signal conditioning

The signal must conform to certain requirements such as frequency band limitation. In addition to this, the way signals will be connected must be addressed, not only does impedance coupling take a big effect, but also the ADC has special requirements which must be met in order to properly digitize analog information. The appropriate high impedance input buffers and anti-aliasing filter were