Materials Science in Semiconductor Processing 11 (2008) 175–178

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

# Silicon nanodot-array device with multiple gates

Mingyu Jo [a], Takuya Kaizawa [a], Masashi Arita [a], Akira Fujiwara [b], Kenji Yamazaki [b], Yukinori Ono [b], Hiroshi Inokawa [c], Yasuo Takahashi [a,*], Jung-Bum Choi [d]

[a] Graduate School of Information Science and Technology, Hokkaido University, Sapporo 060-0814, Japan
[b] NTT Basic Research Laboratories, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi 243-0198, Japan
[c] Research Institute of Electronics, Shizuoka University, 3-5-1 Johoku, Hamamatsu 432-8011, Japan
[d] Physics and Research Institute of NanoScience and Technology, Chungbuk National University, Cheongju, Chungbuk 361-763, South Korea

ARTICLE INFO

Available online 18 January 2009

*PACS:*
73.23.Hk
62.23.Eg
85.35.Gv

*Keywords:*
Single electron
Nanodot array
Coulomb blockade

ABSTRACT

We fabricated a nanodot-array device with multiple input gates on a silicon-on-insulator (SOI) wafer by using a pattern-dependent oxidation method with multiple input gates, which embodies a new concept of a flexible single-electron device. Although the device can generate many logic functions owing to the capacitive coupling between dots and many gates, the complicated structural configuration makes it difficult to confirm the formation of the nanodot array. For further investigation of this kind of device to achieve higher functionality, it is important to demonstrate experimentally that the dot array is actually formed. We analyzed the oscillation-peak shift caused by the gate voltage change, and successfully determined the location of the dots that contributed to the experimentally observed oscillations.



## 1. Introduction

Single-electron devices (SEDs) have been studied as next-generation devices [1–5]. The SED is made of nanodots, and the operation principle, Coulomb blockade, enables the device to control one-by-one electron transfer. The great advantages of the SED are the small size and low power consumption, which are the key issues for highly integrated circuits. In addition, SEDs have two special features: oscillatory current–voltage characteristics as a function of gate voltages and the capability of attaching multiple input gates [1].

Since the SED will be used with a smaller feature size than that of CMOS FETs, the size fluctuation will be more critical. As is well known, the electrical characteristics of SEDs depend on dot size. To overcome size fluctuation, we have proposed a new type of device, which has a nanodot array with multiple input gates [6]. We used many nanodots to compensate for the size fluctuations and used the two special features of SEDs to achieve higher functionality. A schematic top view of the device we fabricated is shown in Fig. 1(a), and its basic experimental operation is demonstrated. Six nanodots are arranged between source and drain terminals, and they are connected to one another by tunnel capacitors. Two finger-structure gates are attached over the dot array and used as input gates of a two input logic gate device, in which the output drain current is modulated by the two input-gate voltages. In addition, another gate, the control gate, is also attached on top of the device to couple capacitively with almost all the dots. The measured drain current $I_d$ versus control-gate voltage $V_g$ characteristics for four combinations of the two input-gate voltages are shown in Fig. 1(b). Elemental logic functions are able to be outputted when we introduced the threshold current to distinguish "high" and "low" output current levels. We obtain the six most important logic functions by analyzing the characteristics [7].

Although this is an experimental demonstration of a new device, this is not a confirmation of the formation of the dot array. All the dots in the device are coupled with almost all the gates, which makes the origin of each

* Corresponding author. Tel.: +81 11 706 6794; fax: +81 11 706 6457.
*E-mail address:* y-taka@nano.ist.hokudai.ac.jp (Y. Takahashi).

1369-8001/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mssp.2008.12.001

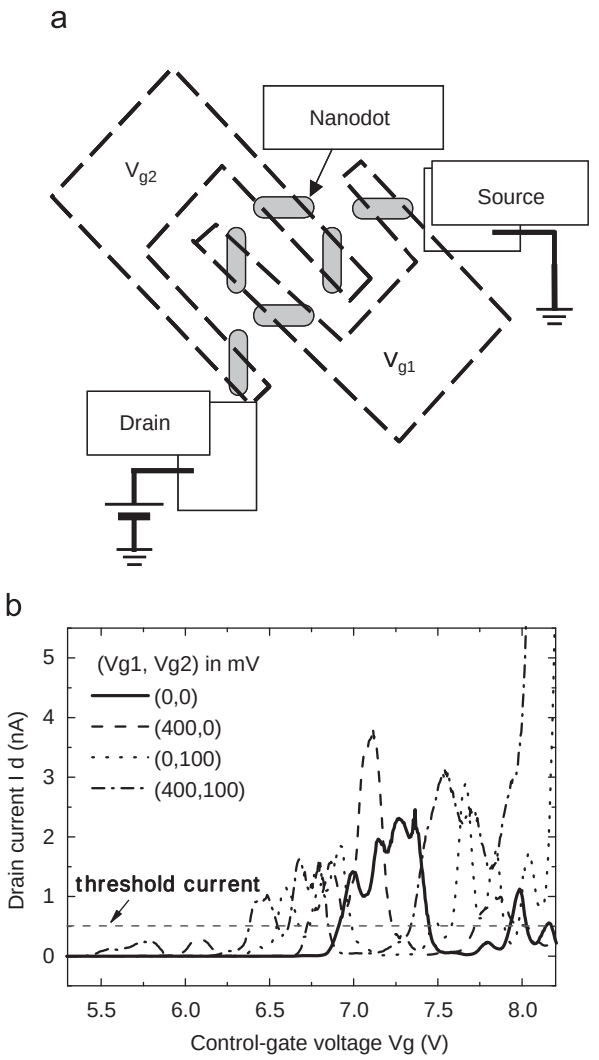


**Fig. 1.** (a) Schematic top view of nanodot array where the control gate covering the entire area is not shown here. (b) The drain current $I_d$ versus control-gate voltage $V_g$ characteristics measured at $V_d = 5$ mV for four combinations of $V_{g1}$ and $V_{g2}$.

oscillation indistinctive. To achieve higher functionality together with low power consumption, we have to expand the array size and the number of input gates. Before making such complicated devices, we need to clarify the formation of a dot array. In this paper, we fabricated another nanodot-array device, which has three input gates, to confirm the formation of the nanodot array. Each of the three input gates is coupled capacitively with few dots, which makes it easy to analyze the origin of current oscillations.

## 2. Experimental details

The device was fabricated on an silicon-on-insulator (SOI) substrate by using conventional Si-CMOS processes. A schematic top view of a fabricated device is shown in Fig. 2. A Si nanowire was formed by electron-beam lithography and dry etching. The wire width, length, and

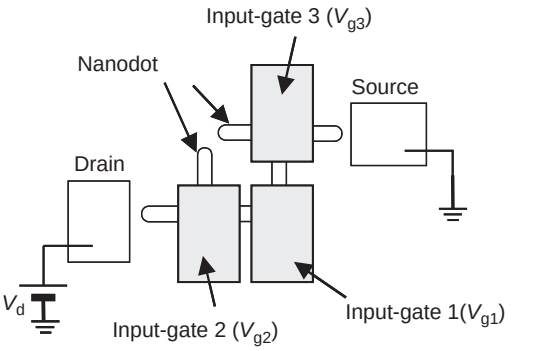


**Fig. 2.** Schematic top view of fabricated devices formed by three input gates to analyze the origin of current oscillations. The control gate covering the entire area is not shown here.

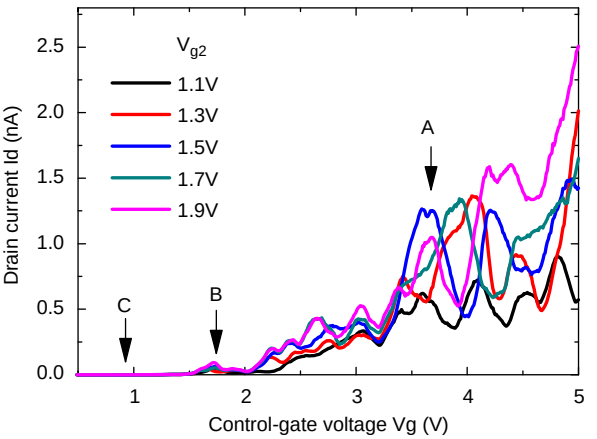


**Fig. 3.** Drain current $I_d$ versus control-gate voltage $V_g$ characteristics measured at $V_d = 5$ mV, $V_{g1} = 2$ V, and $V_{g3} = 2$ V. The parameter is $V_{g2}$, which was changed from 1.1 to 1.9 V at 200 mV intervals. Peaks marked with arrows "A", "B", and "C" are investigated.

height are about 50, 100, and 35 nm, respectively. Then, we employed the pattern-dependent oxidation (PADOX) [8,9] method to convert the wire into a Si nanodot array. Si islands connected by a tunnel capacitor were automatically formed, as shown in Fig. 2. Then, three input gates made of phosphorous-doped polycrystalline-Si were attached on a Si dot array to cover part of the dot array. After $SiO_2$ interlayer deposition, a wide another polycrystalline-Si control gate was formed.

## 3. Results and discussion

Electrical characteristics were measured at 8 K in a low-temperature probe station by the use of an Agilent 4156C precision semiconductor parameter analyzer. $I_d$ versus control-gate voltage $V_g$ characteristics at a drain voltage $V_d$ of 5 mV are shown in Fig. 3. The parameter was one of the input-gate voltages, $V_{g2}$, while the other two input-gate voltages, $V_{g1}$ and $V_{g3}$, were fixed at 2 V. As shown in Fig. 3, complicated oscillations due to the multiple-dot system are also changed in a complicated manner when $V_{g2}$ was changed. However, some of the peaks simply shift toward the lower $V_g$ direction as $V_{g2}$