Materials Science in Semiconductor Processing 11 (2008) 390–393

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Very low leakage InGaAs/InAlAs pHEMTs for broadband (300 MHz to 2 GHz) low-noise applications

A. Bouloukou *, B. Boudjelida, A. Sobih, S. Boulay, J. Sly, M. Missous

School of Electrical and Electronic Engineering, The University of Manchester, P.O. Box 88, Manchester M60 1QD, UK

ARTICLE INFO

Available online 23 January 2009

PACS:
85.35.Be
85.40.−e

Keywords:
pHEMT
InGaAs
Leakage current
Low noise
Noise resistance

ABSTRACT

This paper presents the design, fabrication and characterisation of InGaAs–InAlAs high electron mobility transistors (pHEMTs) suitable for low-frequency LNA designs. Very low levels of leakage, in the order of 0.05 A/cm^2, are demonstrated by the pHEMTs, which have enabled the implementation of large-geometry, low-noise devices. Transistors with gate widths ranging from 200 μm to 1.2 mm are demonstrated to operate up to frequencies of 30 GHz. These are extremely promising as LNA components for implementation in broadband low-frequency systems as the very low-noise resistance simplifies matching requirements. The levels of leakage observed in our transistors further support the potential of the InGaAs/InAlAs material system as an alternative to Si when the CMOS roadmap comes to an end.

1. Introduction

The drive towards ever decreasing device dimensions and its consequent scaling in both vertical and lateral directions, is putting severe pressure on gate leakage currents [1]. This situation is being addressed with the use of high-k dielectric oxides in both CMOS and other advanced III–V alternatives.

The InGaAs–InAlAs pseudomorphic high electron mobility transistor (pHEMT) system occupies a prime position in the microwave and RF fields and is now seriously being considered for CMOS alternatives [2–7]. Its excellent materials properties, however, are impeded by the presence of a relatively large leakage current, which has hampered its use in applications requiring large gate periphery, such as low-frequency radio astronomy applications that have been the initial target of this work.

High-performance receiver applications have historically been implemented using only a few, cryogenically cooled, high-performance HEMTs. In such cases, minimising the noise figure has been achieved through the use of small, typically 0.1 μm, gate-length [8–11] transistors. However, due to the very large number of receivers and wide band requirements of certain systems, one example being the Square Kilometre Array (SKA), research is now focusing on designing less expensive, room temperature-operated LNAs.

The SKA is envisaged to be a unique array-based radio telescope and its design is currently the subject of a large international effort. It is intended to provide an effective collecting area of 1 km^2 and to operate at frequencies from 0.15 to 25 GHz [12]. Covering this frequency range is most likely going to involve two separate antenna technologies for the lower (0.1–2 GHz) and upper (2–25 GHz) frequency bands. In this frequency range, matching the LNA for wide band, low-noise performance becomes a critical design issue as it typically requires the inclusion of large passive components that can either be integrated on-chip, acting as a source of added noise in the LNA, or implemented as off-chip components [13], increasing the overall cost. To make an MMIC LNA that is insensitive to matching across the entire band requires the use of active devices that simultaneously exhibit a low noise figure (NF) and a low noise resistance (Rn). Small gate-length InGaAs/InAlAs

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* Corresponding author. Tel.: +44 161 306 4776; fax: +44 161 306 4802.
E-mail address: a.bouloukou@manchester.ac.uk (A. Bouloukou).

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doi:10.1016/j.mssp.2008.11.006

pHEMTs are the best candidates for achieving very low NFmin. However, the relatively high leakage currents in this material system become even more pronounced as dimensions shrink and thus prevent the use of very large periphery devices, which are needed to reduce Rn.

We report here on novel InGaAs/InAlAs pHEMTs that have been designed for use in the SKA and fabricated using conventional optical lithography. Precise material engineering of the epilayers and doping profile result in on-state leakage of $I_g = 0.05\,A/cm^2$. This low leakage enables very large periphery devices (up to 1.2 mm gate width (W_g) and 1 μm gate length (L_g)) to be fabricated.

2. Process technology

The pHEMT structure under investigation (wafer XMBE109) was grown, in-house, using solid-source molecular beam epitaxy (MBE) on an Oxford Instruments V90H system. It is based on an InGaAs/InAlAs/InP epitaxial layer design and consists of an InAlAs buffer, strained InGaAs channel, δ-doped InAlAs supply and undoped InGaAs cap layer, as shown in Table 1. The Hall mobility and 2-DEG sheet carrier concentration for this sample were $12{,}900\,cm^2/V\,s$ and $1.75 \times 10^{12}\,cm^2$ at room temperature, respectively.

Devices were fabricated by first defining isolated mesas by means of wet-etching down to the InAlAs buffer layer, using a non-selective etch (H_3PO_4:H_2O_2:H_2O). Source and drain Ohmic contacts were formed through thermal evaporation and lift-off of AuGe/Au. The gate recess was subsequently formed in a self-aligned process, using the gate-level photoresist opening as a mask. A highly selective adipic acid etch [14] was used to remove the InGaAs cap layer and form the 50 Å gate recess. The gate electrode was deposited by thermal evaporation and lift-off of Ti/Au. Ti/Au probe pads were deposited to improve the Schottky contact and enable microwave probing for on-wafer RF measurements. Airbridges were fabricated to act as source level interconnects for the multi-finger transistor and are formed through Au evaporation and lift-off.

3. Results and discussion

3.1. DC characteristics

The transistors were fabricated with a gate length of 1 μm. Typical room temperature characteristics are shown in Fig. 1. The device exhibits good output characteristics with a knee voltage of 1 V and an off-state breakdown voltage of over 15 V. The low field source–drain resistance of this device is 2.16 Ω mm, for a source–drain separation of 5 μm and an Ohmic contact resistance of 0.18 Ω mm. The Schottky diode characteristics of the device yield an ideality factor of 1.28 and barrier height of 0.61 eV.

Table 1
Epitaxial structure of the InGaAs/InAlAs pHEMT.

Cap	$In_{0.53}Ga_{0.47}As$	5 nm
Barrier	$In_{0.52}Al_{0.48}As$	30 nm
δ-Doping	Si	–
Spacer	$In_{0.52}Al_{0.48}As$	10 nm
Channel	$In_{0.7}Ga_{0.3}As$	16 nm
Buffer	$In_{0.52}Al_{0.48}As$	450 nm

2 in S.I InP substrate.

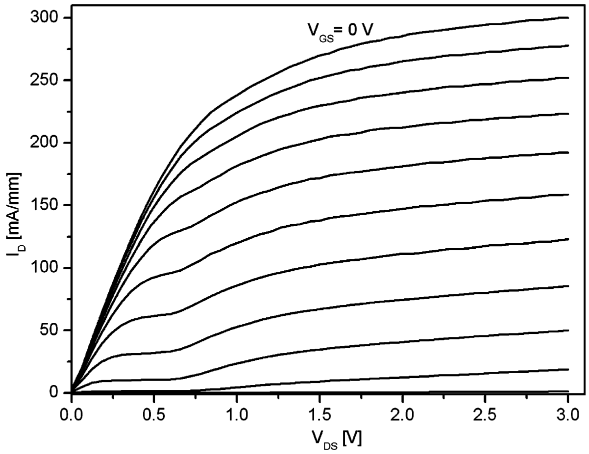

Fig. 1. Typical room temperature, transistor output characteristics ($L_g = 1\,\mu m$, $W_g = 200\,\mu m$, V_{GS} step $= -0.13\,V$).

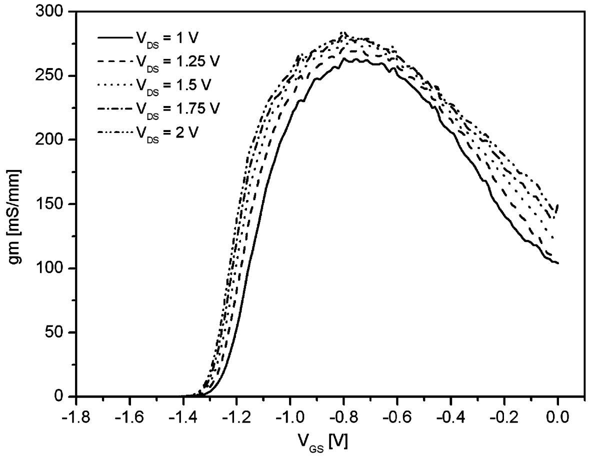

Fig. 2. Typical transconductance characteristics ($L_g = 1\,\mu m$, $W_g = 200\,\mu m$).

Figs. 2 and 3 show the transfer characteristics of the transistor at various bias points. The peak transconductance (g_m) of this device is 280 mS/mm at $V_{GS} = -0.79\,V$. The on-state leakage current peaks at approximately $V_{GS} = -1\,V$ and ranges from 0.6 to 15.7 μA/mm for $V_{DS} = 1$ and 2 V, respectively. The characteristic bell-shaped curve of the leakage is associated with the hole current due to impact ionization. Minimal contribution of reverse leakage due to tunnelling is observed. The leakage level is 60 times lower than that reported in [15] and attests to the very low leakage currents exhibited by the new pHEMT epitaxial design. Such low levels of gate leakage indicate that it is possible to use large-geometry devices, commonly employed in high-power applications, for low-noise operation.