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Experimental characterization of low-frequency noise in power MOSFETs for defectiveness modelling and technology assessment

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ABSTRACT

In this work we analyse the applicability of low-frequency (LF) noise measurement in order to study the defectiveness in the gate oxide of power MOSFETs (Metal–Oxide–Semiconductor Field-Effect Transistors). To this purpose, we implement a low-noise experimental set-up, which is able to measure, in particular, the flicker ("1/*f*") contribution to the drain noise current of the device under test, with high accuracy in terms of noise floor and the adequate bias system flexibility required by the application. First, we show how these measurements can be used to empirically detect the physical model and related compact expressions, which best describe the source of 1/*f*-like fluctuations in this type of devices. Then, according to the selected physical model, the defect density in the gate oxide is extracted. In order to validate the proposed methodology, experimental data are reported and discussed in the case of power U-MOSFETs.

1. Introduction

The bias- and frequency-varying experimental characterization of noise performance of electron devices is a largely adopted, common measurement activity for the extraction of circuit-oriented empirical noise models, usually devoted to the CAD of low-power circuits (e.g., low-noise amplifiers, low phase-noise voltage-controlled oscillators, etc.). However, low-frequency (LF) noise measurement represents a powerful tool to also investigate, from an empirical standpoint, the reliability (process defectiveness, stress-induced degradation, etc.) of semiconductor devices [1–3]. Its usefulness was largely proved in the field of CMOS devices with the aim of studying the impact of the technological parameters and adopted materials on the overall gate stack quality [4–6]. In particular, the drain current flicker (1/*f*) noise was shown to be related to the defects located at both the silicon-oxide interface and within the gate oxide [4]. These defects are responsible for dispersion effects and significantly influence the reliability of the devices. Therefore the estimation of this phenomenon represents an useful assessment for MOSFET technologies. Flicker noise was also studied in [7,8], regarding discrete power MOSFETs, aiming at investigating the effect of ionizing radiation on drain current noise, although without modelling the current fluctuations. In [9–11], 1/*f* noise was analysed in Laterally Diffused MOS (LDMOS) to investigate the effect of stress [9,10] and of the drift region [11].

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In our previous works [12–14] we developed a compact analytical model for the gate current flicker noise, which was validated on CMOS devices. Furthermore, in [15,16] we demonstrated the suitability of LF noise investigation to analyse the impact of high-k materials exploited as gate dielectric in CMOS technology. To this purpose, drain current flicker noise was measured and compared when considering different gate stack architectures.

In this work, we implement an experimental set-up for LF noise measurement in vertical power MOSFETs. The LF noise analysis has a twofold purpose: (i) to select, among those provided by the literature, the physical model which most suitably describes the source of LF fluctuations for the technology considered, by comparing its analytical predictions to the empirical evidence; (ii) on the basis of the compact physics-based model equation selected and validated through the experimental data, to estimate the defect density in the gate oxide of the device under test (DUT). Since the compact equations of the physical models available in the literature mostly correlate LF noise to DUT defectiveness on the hypothesis that the device is biased in linear region, in which a uniform channel under the gate is present, the application considered in this work requires the biasing of the device under such DC operating conditions, in order to correctly exploit the experimental data collected. Therefore, in this work we will discuss the adoption of the experimental set-up to analyse the LF noise of vertical power MOSFETs in linear region only.

Since vertical power MOSFETs typically have very large channel width, flicker noise is expected to be very low when compared to the noise levels associated with other MOS technologies devoted to lower power applications. Hence, the minimization of the noise floor at the measurement section is a first, fundamental criterion to be considered in the design of the set-up, followed by an accurate experimental assessment that the goal has been actually achieved. Low injected noise, high resolution and flexibility in the biasing at the gate port are further essential requirements, as discussed in details in Section 3.

The paper is organized as follows: in Section 2 we discuss the equivalent circuit noise model adopted for a power MOSFET; in Section 3 the architecture and the design guidelines of the low-noise experimental set-up are described, along with experimental data regarding its characterization; in Section 4 we report an example of application involving silicon power U-MOSFETs (also referred to as trench-gate power MOSFETs); finally, in Section V the main conclusions of this work are drawn.

2. Equivalent circuit-based noise model of a power MOSFET

The characterization technique discussed in this paper requires (for the particular application described in Section 4) the experimental evaluation of the LF noise at the drain electrical port of the device. From a general, circuit-oriented standpoint, the noise properties of a power MOSFET can be analysed by considering a *noiseless* representation of the device, suitably connected to the gate and drain short-circuit noise current equivalent generators. More precisely, Fig. 1a shows the equivalent circuit noise model adopted in the following for a generic power MOSFET: the ideal noiseless device (i.e., not affected by any stochastic phenomena) is considered and two bias-dependent noise current generators are applied at its ports as shown, in order to equivalently account for the gate and drain current fluctuations, which are instead experimentally observed. In particular, in Fig. 1a, the generators are referred to by the corresponding noise current (one-sided) power spectral densities (PSDs) G_{ig} and G_{id}. The gate and drain bias networks, which are needed in order to operate the device under specific bias conditions, introduce two equivalent impedances, Z_{GB} and Z_{DB}, respectively. Since the considered application is based on the evaluation of the noise at a single port, i.e., the drain-source terminals, under bias-varying quiescent operating conditions, it is then useful to consider the Norton equivalent network of Fig. 1a (Fig. 1b), in which R_{ch} is the small-signal channel resistance of the power MOSFET calculated for the given bias point, and the PSD G'_{id} corresponds to the single equivalent noise current generator resulting from the above mentioned circuit transformation, expressed as:

$$G'_{id}(f) \cong G_{id}(f) + |Z_{GB}(f)|^2 g_m^2 G_{ig}(f) - 2g_m \sqrt{G_{ig}(f) G_{id}(f)}\,\mathrm{Re}\{Z_{GB}(f) C_{ig,id}(f)\} \quad (1)$$

g_m being the transconductance of the power MOSFET and $C_{ig,id}$ the complex correlation coefficient between the gate and drain current fluctuations introduced in Fig. 1a. Although the PSD (1) of the short-circuit noise current shown in the Norton equivalent of Fig. 1b suffers from a contribution due to the propagation of the gate noise through the device, nevertheless this effect can be neglected in the present application. Indeed, due to the thick gate oxide of power MOSFETs the DC current I_G is typically very low, and this leads to a reduced gate noise current spectrum G_{ig} (for shot, flicker and generation-recombination components), which is negligible with respect to G_{id} even after the gate-to-drain mild amplification. Under this hypothesis, we can assume $G'_{id} \cong G_{id}$ in the following, as far as the overall noise introduced by the device itself is concerned. However, the gate bias network also introduces an open-circuit equivalent noise voltage $G_v^{(GB)}$ at its output (see Fig. 1a), which must be accounted for as a further possible perturbation on G'_{id}:

$$G'_{id}(f) \cong G_{id}(f) + G_v^{(GB)} g_m^2 \quad (2)$$

The actual implication of $G_v^{(GB)}$ on noise measurement accuracy is discussed in Section 3, where further details about the gate bias network are provided.

3. The experimental set-up for LF noise measurement

3.1. Architecture

The experimental set-up designed and implemented in this work, which derives from a refinement of the architecture exploited in [17] and has been preliminary discussed in [18], is shown in Fig. 2. The drain port of the DUT is connected to the high-impedance input of a pre-amplifier