Measurement 54 (2014) 191–200

Contents lists available at ScienceDirect

Measurement

journal homepage: www.elsevier.com/locate/measurement

A portable measurement system for power profiling of processing units

F. Picariello *, S. Rapuano, U. Villano

University of Sannio, Corso Garibaldi 107, Palazzo dell'Aquila Bosco Lucarelli, 82100 Benevento, Italy

ARTICLE INFO

Article history:
Available online 4 January 2014

Keywords:
Benchmark
Workstation computer
Data acquisition system
Power consumption
Measurement system

ABSTRACT

The paper deals with the design and the metrologic characterization of a portable power consumption measurement system capable to correlate the average power consumption of a central processing unit to processor performance. A survey of power measurement systems designed for the evaluation of computer energy performance is provided. The design steps for the proposed power measurement system and its comprehensive hardware and software descriptions are reported. Furthermore, a calibration procedure of the power measurement system is described. Five benchmark tests have been executed on an Intel Pentium D processor and the measured power loads are reported and discussed.

1. Introduction

Nowadays, processor architectures are designed for optimizing both performance and energy efficiency, especially for mobile applications, where the battery life is an important issue. The processing requirements of battery-powered systems are increasing faster than battery storage capacity. Since large and heavy batteries are unacceptable for handheld computers, low-power designs and smart power management are crucial for these systems [1]. In the case of consumer electronics equipment, and especially for mobile phones, battery storage capacity is restricted, due to constraints on size and weight of the devices. This implies that energy efficiency has a relevant impact on the portability of such equipment [2]. Furthermore, high power consumption is undesirable for workstation computers, being the cause of acoustic noise and computer overheating. For these reasons, the processors design trend is oriented to multiple core devices operating at relatively low frequency, which can provide an increase of computational speed while reducing power consumption, as compared to the previous generation of high-speed single core processors. Moreover, modern processors also include low-power consumption states. To take advantage of such feature, the operating system has to put the processor in this low-power state every time that it turns out to be idle. In [3], several algorithms to allow the transition to the low-power state are reported. The mentioned paper points out that the Central Processing Unit (CPU) is one of the major power consumers in a computer system, and that the design of processor architecture and software management have an essential role for the reduction of the power consumption.

As for the architecture of every single core of modern CPU, it can be observed that, over the years, the architectures are becoming more and more complex. Also at this level, the key is to increase processing performance while at the same time taking into account power consumption. All recent CPUs for high-performance workstation computers are based on superscalar design. These processors rely on duplicated independent functional units that execute instructions in parallel. Parallelism and pipeline processor architectures have a direct impact on processor designs. Highly parallel processors, in fact consume, more power than non-parallel ones and deeply pipelined functional units consume more power than non-pipelined ones. These suggest several tradeoffs between power consumption and processor architecture organization [4]. During the design

* Corresponding author. Tel.: +39 3881966423.
E-mail addresses: fpicariello@unisannio.it (F. Picariello), rapano@unisannio.it (S. Rapuano), villano@unisannio.it (U. Villano).

0263-2241/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.measurement.2013.12.040

of such processors, the designers use complex emulation software in order to estimate the power consumption and processing performance [5]. This emulation software is based on behavioral models of the processor core, and so it has an intrinsic made uncertainty. For this reason, benchmarks for estimating both processor computational capabilities and power consumption are necessary and widely used during the design and test phases. In order to compare the CPU models, it is necessary to correlate the processing performance of microinstructions (e.g., cache misses, mispredicted branches, number of active threads, page faults and use of floating point unit, and so on) to the power consumption of the processor. However, the power consumption can be measured only through the use of external power measurement systems, because a core processor does not include embedded ones.

In [1,6,7], several key power measurement systems designed to evaluate the power performance of processors are presented. The proposed power measurement systems use oscilloscopes or multimeters, which measure the current consumption using shunt resistors or Hall-effect based sensors. These systems have several disadvantages: (i) they are bulky (e.g., large size of the used instruments), (ii) they are not portable, and (iii) the current measurements cannot be traced back to the International System of Quantities because calibration procedures are not available and so the system is not referable to a reference measurement instrument. Nowadays, it is possible to design portable power measurement systems that can be integrated directly on the computer case providing referable measurements. By taking into account the stated reasons, the long-term target of the research described in this paper is to design a portable power measurement system, which provides characterization of processor energy performance by means of direct power measurements from the motherboard connector of the processor under test (PUT). This system should manage the benchmark execution on the PUT, and at the same time measure its power consumption. The output of the system should be the power consumption for each processing performance result provided by the benchmark. To this aim, this paper presents the design of a portable measurement system for measuring CPU power consumption. Besides this, the first results linked to the use of our measurement system are documented here, namely: (i) the study of the power in the time and frequency domains, (ii) the definitions of the measurement system requirements (for the voltage and current transducers) and the measurement system architecture, (iii) the measurement system prototyping, and (v) the measurement system characterization. The availability of the measurement system makes it possible to correlate the measurements of power consumption to the on-going CPU activities, running benchmark tools that also provide the corresponding processor performance. As far as our power/performance measurements are concerned, the most popular benchmarks have the following disadvantages: (i) they do not allow to execute a task in every available processor core, (ii) they provide processor performance with metrics that are not standardized, and (iii) the average performance is evaluated over unknown time intervals. One of the effects of these disadvantages is a reduced repeatability of the results provided by the benchmarks.

This paper is focused on: (i) the design of a power consumption measurement system, which is compact, referable, and configurable, and (ii) its use for analyzing the relationship between the obtained power consumption measurements and the performance measured using several different kinds of benchmarks, in order to discover the codes that lead to higher power consumption, and possibly avoiding them if low power consumption is an issue. The paper is organized as follows. Section 2 includes an overview of the power measurement systems existing in literature. Section 3 deals with the general proprieties of benchmark used for the performance analyses and with a description of the used benchmark tool. The measurement requirements of the proposed power measurement system are presented in Section 4. The hardware and software descriptions and the metrological characterization of the proposed portable power measurement system are presented in Section 5. In Section 6, the results of power consumption measurements running five different benchmark tests on an Intel Pentium D processor are shown. Finally, our conclusions are drawn.

2. Related work

Current literature provides several papers dealing with the power consumption measurements during the execution of workloads. These workloads are usually produced by running suitable benchmarks. These are specially designed to provide information about processor performance during the execution of assigned software tasks. In this way, it would be possible to correlate the power consumption to the computing performance of the PUT.

However, the only measurement directly available from the majority of general-purpose processors is the temperature of the CPU chip. This measurement cannot be used for estimating power consumption, because it depends by: (i) the positioning of the sensor on the chip, and (ii) the cooling system used. Consequently, to obtain reliable power consumption measurements it is necessary to use an external power measurement system. This almost inevitably consists of current and voltage transducers placed on the power supply rails of the PUT.

In [1], the authors measure the power consumption of the Itsy pocket computer in order to compare several low-power design optimizations and power management strategies. The authors measure the total average power consumption and the power dissipated by six sub-circuits of the Itsy pocket computer during the execution of seven benchmarks. The proposed power measurement system consists of seven multimeters and seven shunt resistors. The average power consumption and computing performance of five processors during the execution of 61 benchmarks are instead presented in [6]. For each processor, the average power consumption was evaluated in several processing configurations (single and dual cores, single and dual threads). The power measurement system described in [6] consists of a Hall Effect Current Transducer (HECT) connected to the power supply rails