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Correlated full-field and pointwise temporally resolved measurements of thermomechanical stress inside an operating power transistor

Dan N. Borza*, Christophe Gautrelet

Normandie University, INSA Rouen, LOFIMS, 13 Avenue de l'Université, F-76801 Saint-Etienne du Rouvray, France

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ABSTRACT

The paper describes a measurement system based on time-resolved speckle interferometry, able to record long series of thermally induced full-field deformation maps of die and wire bonds inside an operating power transistor. The origin of the deformation is the transistor heating during its normal operation. The full-field results consist in completely unwrapped deformation maps for out-of-plane displacements greater than 14 μm, with nanometer resolution, in presence of discontinuities due to structural and material inhomogeneity.

These measurements are synchronized with the measurement of heatsink temperature and of base-emitter junction temperature, so as to provide data related to several interacting physical parameters. The temporal histories of the displacement are also accessible for any point. They are correlated with the thermal and electrical time series.

Mechanical full-field curvatures may also be estimated, making these measurements useful for inspecting physical origins of thermomechanical stresses and for interacting with numerical models used in reliability-related studies.

1. Introduction

Electronic and mechatronic devices are often subjected to harsh operating conditions which may influence their reliability and finally lead to failure. Increasing miniaturization and working frequencies, high current and dissipated power, embedding of electronic devices, large variations of external temperature, the presence of moisture and vibrations impose new design concepts allowing power components to withstand these conditions and high thermomechanical stresses.

Finding the root causes of a device failure is an important step towards improving reliability and introducing new concepts in the design of products. For this reason electronic component failure analysis is important for the improvement of device quality.

These root causes are extensively presented by Blackwell [1]. The physics-of-failure lifetime prediction models pointed out the incorrect packaging and mounting as an important factor. It is studied in many publications, amongst which are Refs. [2,3]. Other important causes are the electrical and thermal operating conditions going above safe operation specified by the manufacturer. At board and package levels, some causes of failures are investigated in [4,5]. Yu et al. [6] stated that the first root causes of electronic package failure are drop impact, vibration and thermal cycling. For the rest of this paper, the discussion will be limited to mechanical stress of thermal origin generated by the power dissipated in some internal parts of the power device, such as the wire bonds.

Some of the most stressed parts in a power transistor or in an integrated device are the interconnections between the semiconductor device and its packaging. A plethora of researchers and papers studied this subject. The interconnections are most often realized by wire bonding, by ribbon bonding or with solder bumps [7]. Wang and Sun [8] showed that the reliability of the IC chip during operation is depending on the quality of the wire bond interconnection. They discussed in detail some testing methodologies, such as the bond pull test, the bond shear test and visual inspection. Servais and Brandenburg [9] presented information on the ability of a bond to withstand different aging conditions. They proposed an effective way to control bond quality. Hu et al. [10] analyzed some various thermo-mechanical damage mechanisms during the wire bond operation. The thermo-mechanical deformation in electronic packages may be studied on theoretical, numerical or experimental basis. An example of study achieved on a theoretical basis is presented in [11] by Beom and Jeong. Out-of-plane and in-plane deformations due to thermal strain mismatch are estimated using the laminated plate theory and presented as functions of the layer geometries and material properties.

Takahashi and Inoue [12] established, by using a numerical approach, a relationship between the bondability and the interfacial

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[*] Corresponding author. Tel.: +33 232 959 742, +33 232 959 761.
E-mail addresses: borza@insa-rouen.fr (D.N. Borza), christophe.gautrelet@insa-rouen.fr (C. Gautrelet).

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deformation. The numerical simulation, made on the basis of very large deformations, allowed visualizing the interfacial contacting process which occurs for several ms. In 2013, the authors of Ref. [13] presented an extended review of most well-known physics-of-failure-based life prediction models for wire bond interconnects. The results of the experimentation suggest the necessity of new approaches to wire bond life prediction models. The authors of paper [14] found experimentally that bond wire heel crack failures are strongly dependent on the loop geometry. Based on this theory they derived an improved finite element model that accounts for elastic–plastic material properties. Numerical modeling is often used to predict the effects of the operating conditions on reliability. In [15], the thermal modeling of a power transistor is made for two different configurations, with and without heatsink. The simulation allows estimating the temperature of the case. The same subject is discussed by Meyyappan [16], the main accent being put on the failure mechanisms of wire bonds due to wire flexure. Several other failure mechanisms were identified, such as wire bond lift-off, cracking, corrosion and electrical leakage. The cracking of wire bond joints, modeled by finite elements [17], allowed simulating the failure mechanism and the initiation and growth of cracks.

Experimentation and testing allow inspection of the physical origins of thermomechanical stress, an essential task for improving the numerical modeling and reducing the risks of failure. It allows a phenomenological analysis and takes into account practical data related to the physical behavior of structures and materials inside a microelectronic device.

Some of the most interesting quantities being measured are the temperature of semiconductor junction and of heatsink, the full deformation and strain fields of the whole device or of some key parts of it – most often wire bonds and die. Simultaneous, synchronous measurement of these quantities may bring essential information for the estimation of device reliability.

The techniques used for testing are based on various principles: electrical, thermal, acoustical, optical – as well pointwise as full-field. There is an impressive number of books, journal papers and scientific conferences covering various subjects related to testing of individual electronic components and of assembled PCB. Some of these techniques will be briefly mentioned here. The main interest of this paper is the full-field measurement coupling a high spatial resolution with a high temporal resolution with temperature and voltage measurements. The displacement measurement has an extended measurement range and may cope with large and discontinuous displacement fields. The low level of noise allows estimating the curvatures across the object surface.

Several optical full-field displacement measurements may be used for testing electronic components and systems: microscopy, projection moiré and moiré interferometry, 3d measurement by line projection, digital image correlation [18], holographic interferometry, digital holography, and speckle interferometry (out-of-plane, in-plane, shearography). Some of these techniques (projection moiré, 3d measurement by line projection) use non-coherent light, eventually video projectors, and they are performing well in measuring very large displacements (mm, cm). Some other use coherent light. The most often used techniques are moiré interferometry [19–21], holographic interferometry, digital holography, and speckle interferometry (out-of-plane or in-plane speckle interferometry, shearography) [22,23]. Their sensitivity is higher (a fraction of light wavelength). Digital holography and its applications in testing are exposed by Schnars and Jueptner [24], by Asundi [25] and by Picart and Li [26]. Digital holography makes use of great progress in digital computing and is efficient since it may produce a high spatial resolution wrapped phase map across the object surface using just a single specklegram, instead of a group of three or four phase-stepped specklegrams. It may thus be recommended for dynamical applications.

Full-field speckle interferometry uses a CCD or CMOS camera and has high spatial resolution. Since these techniques are interferometric they have a high displacement sensitivity, around $10E-2$ µm; their measurement range is usually limited to a few µm. Apart from the contributions presented in the literature by some producers of commercial speckle interferometry systems, the number of contributions to this field from the academic world is rather limited.

In papers [27,28], the authors describe the electronic speckle pattern interferometry as used in their laboratory in the nineties. It was applied to the thermomechanical study of a MOS power transistor. The steady state deformation is measured using full-field ESPI, while the temporally transient regime is obtained pointwise by using a Michelson interferometer.

An important contribution was made by Avery and Lorenz [29], dealing with the in situ measurement of wire-bond strain in electrically active power semiconductors by out-of-plane and in-plane speckle interferometry. They tried to overcome the problem of displacement discontinuities between emitter wire-bound and die by drawing a contour around the wire-bond, then unwrapping only the region inside this mask. The most important features of the thermomechanical deformation inside a power microdevice addressed by Avery and Lorenz are unwrapping the full-field displacement maps, thermal modeling and the use of a thermal camera for obtaining the full-field temperature distribution.

The use of a laser as light source is introducing speckle noise in the result of the measurements – the modulo 2pi wrapped phase patterns. Speckle noise and speckle decorrelation are limiting the total number and the spatial density of fringes and create great difficulties in unwrapping the phase maps. Unwrapping difficulties are highly increased by discontinuities in the fringe patterns, as in the case of the heterogeneous inner structure of a power device. Other limiting factors are the lack of temporal information allowing to follow simultaneously the temporal and the spatial modifications of the deformation map and the lack of synchronized information related to the local temperature in different locations inside the power device. Overcoming these limitations may help in applying the physics-of-failure (PoF) approach, one of the reliability prediction methodologies [30].

The present paper intends to extend other authors' findings and describe a measurement system able to provide accurately

- the temporal evolution of the full-field out-of-plane displacement-related phase maps;
- the complete spatio-temporal discontinuous phase unwrapping, up to displacements of more than 10 µm, without post-processing for masking individual parts of the structure;
- the possibility to choose, for arbitrary placed points, the local time histories of displacement, in synchronism with pointwise measurements of heatsink temperature, base-emitter junction temperature, V_{BE}, V_{CE} and I_C;
- low noise unwrapped phase maps allowing estimating curvatures by differentiation of full-field displacement distributions.

2. The measurement system

In this section a measurement system is described which is able to acquire data allowing a detailed physical insight on the behavior of microelectronic power devices under thermal stress produced power cycling. The aim is to dispose detailed knowledge allowing developing high power components and predicting their reliability. In particular, the main interest is the full-field measurement of mechanical deformation of the wire bond interconnection