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A novel and low-cost multi-stage approach for the fabrication of silicon nano-structures

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ABSTRACT

A new multi-stage technique for the fabrication of arrays of silicon nano-structures is introduced; the growth mechanism of the developed nano-structures is investigated. In this technique, surface of silicon wafers were textured using anisotropic etching method to generate pyramid structures. The textured surfaces were then etched by electrochemical anodic etching. During anodic electrochemical etching in HF solution, the etching initiated at the edge of the pyramids and progressed inward through the faces. The four 1 1 1 faces of the pyramids etched forming a pore at each face. To develop the nano-structures, at the final fabrication stage, the interconnected walls have been etched using NaOH. Results show that the tip of pyramids corresponds to the tip of nano-structures. A good correlation between the number of pyramids per unit surface area and that of the nano-structures was observed. It was also observed that the nano-structure formed only for high pyramid surface coverage. The effect of anodic electrochemical parameters such as current density and etching time on the fabrication of the silicon nano-structure was investigated. Longer electrochemical etching resulted in thinner interconnect walls, needing shorter NaOH etching time to form and reveal the nano-structure array.

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1. Introduction

Electrochemical etching of silicon in HF solution has attracted a great attention for the fabrication of various micro-structures such as porous silicon [1], trenches [2], and pillars [3,4]. Recently, fabrication of one-dimensional n-type silicon nanowires from porous silicon has been developed using photo-assisted electrochemical etching [5]. This fabrication method uses oxidation and/or wet etching as post-processing techniques leading to the creation of pillars and nanowires.

In order to pre-determine the location of the fabricated silicon nanowires, in the conventional method, the silicon surface is first patterned using lithography technique followed by wet etching [6,7]. This technique leads to the creation of inverted pyramids on the silicon surface followed by the formation of porous silicon starting at the pit of these inverted pyramids.

In this work, a new non-lithographical method was used for the fabrication of silicon nano-structure arrays. In this approach, the pyramid shape seeding points were first created on the surface of the silicon. Each of these pyramids will become the tip of the silicon nano-structures created in the subsequent fabrication stages. However, the anisotropic etching creates randomly distributed pyramids on silicon surface; the position of the created nano-structures in the subsequent fabrication stages is pre-determined by the location of these pyramids. This method of synthesizing silicon nano-structure arrays is appealing because the process is non-lithographic and can lead to a low-cost route for fabricating micro/nanoelectronic devices.

The detail studies on growth mechanism of the nanowires helped develop methods to control the array density and nano-structure size characteristics. To the best of our knowledge this is the first report of implementing the electrochemical anodic etching on the textured pyramids surface with no lithography technique aimed at fabrication of silicon nano-structure arrays.

The influence of NaOH fine-etching time on the morphology and geometry of the nano-structure arrays was investigated in our previous work [8]. Here we report the impact of anodic electrochemical conditions and pyramid surface coverage on the fabrication of silicon nano-structure array.

2. Experimental procedure

Silicon wafers with (1 0 0) orientation (10–20 Ω cm) were purchased from Silicon Inc. and were used for all experiments. All experiments were carried out on p-type silicon, so that, due to the existence of hole majority carriers, no illumination of the sample is required. All samples were cleaned prior to experiments using the RCA process [9]. 25 wt.% tetramethylammoniumhydroxide (TMAH)

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was purchased from Sachem Inc. and diluted with DI water to reach the desired 1.5 wt.% concentration used in all experiments. 99% isopropyl alcohol (IPA) was purchased from VWR International and added to the etching solution to obtain 1.5 wt.% and 6 wt.% weight concentrations. 99.5% ethanol, and 97+% NaOH were purchased from Sigma–Aldrich. 48.8% HF was purchased from ACP Chemicals Inc. Canada. The anodic electrochemical etching was performed using Allied Research galvanostat potentiometer. The developed nano-structures were characterized using Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). The population density of structures and surface coverage measurements were all obtained by performing image analysis of the SEM photos using Image J image processing program developed by the US National Institute of the Health.

This novel approach requires three stages of fabrication to create the desired nano-structure array. The three stages are as follows:

1. Anisotropic wet etching to create textured silicon surface.
2. Anodic electrochemical etching of the textured silicon to create a porous layer.
3. Fine-etching of porous silicon layer to achieve the desired nano-structure array.

2.1. The fabrication process flow

2.1.1. Fabrication of the pyramids (1st stage)

Surface of a 1 cm^2 samples of silicon wafer were textured using anisotropic etching process in 1.5 wt.% TMAH for 30 min. Pyramids with various sizes were developed on the surfaces of the samples. During the process IPA was added to TMAH solution in order to remove the hydrogen bubbles from surface of the sample faster to facilitate the etching process. As we have reported in the earlier work, the concentration of the added IPA will influence the size and surface coverage of the pyramids [10]. In this stage we have used samples etched in TMAH with added various IPA concentrations (0, 1.5, and 6 wt.%). The samples were used to study the effect of pyramids concentrations on the developed final nano-structures.

2.1.2. Creation of porous silicon (2nd stage)

An anodic electrochemical etching was performed on the textured silicon surface to create a layer of porous silicon. The etching was done in a two-electrode Teflon cell with metal base plate to form a back ohmic contact. A thin layer (~1 μm) of aluminum was deposited on the back side of the silicon wafer to obtain an ohmic contact. The silicon wafer is served as working electrode (anode) and the platinum mesh served as counter electrode (cathode). Experiments were performed with various anodic current densities and etching time in such a way that the total charge participating in the reaction, Q, was kept constant at 144 C/cm^2. Q can be calculated by multiplying the current density (0.08 C/s-cm^2 = 0.08 A/cm^2) times the etching time (1800 s). Therefore, two parameter values that affect this total charge are (1) the current density, and (2) the etching time. In order to keep this charge constant, if the value of one parameter increases then the other parameter value must decrease and vice versa. The etching solution (electrolyte) consisted of 1:3 (HF:ethanol) mixture for all experiments. Ethanol was added as a surfactant to facilitate the detachment of the hydrogen bubbles from the surface of the silicon, therefore, resulting in the formation of a more uniform porous layer.

2.1.3. The creation of silicon nano-structure array (3rd stage)

Alkaline solution, consisting of a diluted NaOH (0.2 M), was used to fine-etch the porous silicon layer in order to achieve the desired nano-structure. In this fabrication stage, the walls connecting the pillars in the porous silicon were etched until the desired nano-structure array was achieved. A few drops of IPA were applied to the surface of the sample (porous silicon) to increase its wet-ability before immersing it into the NaOH solution. The temperature was kept constant at 35 °C, and some agitation was applied using a magnet stirrer.

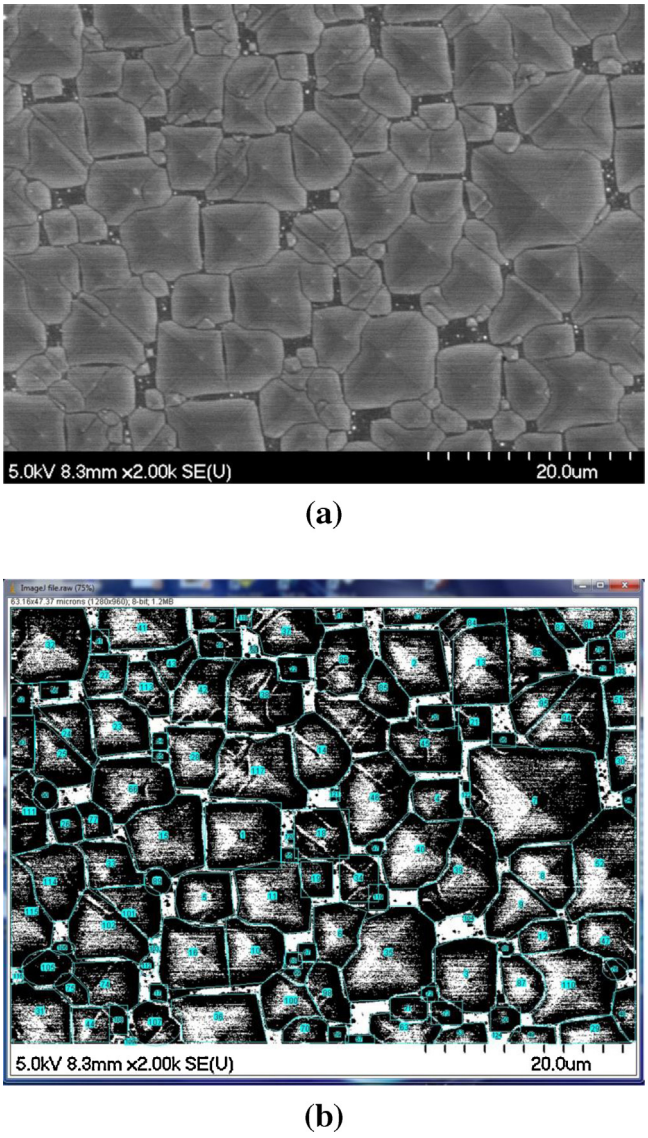

Fig. 1. (a) Textured silicon surface and (b) image analysis of the textured silicon surface.

3. Results and discussion

3.1. Characterization of the textured silicon surface

Samples with different pyramid surface coverage (during the first stage of anisotropic etching) were achieved as a result of various IPA concentrations. Fig. 1(a) illustrates the SEM image of a sample textured using 1.5 wt.% concentration for IPA (high surface coverage). Fig. 1(b) illustrates the use of image analysis of SEM image to calculate the surface coverage and the number of pyramids per unit area.

Table 1 summarizes the influence of various IPA concentrations on the resulting pyramids surface coverage and the number of pyramids per unit area. In order to obtain an average of the measured values, the same experiment was repeated a few times. As it may

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