Sensors and Actuators A 165 (2011) 101–106

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

Multi-layer atom chips for atom tunneling experiments near the chip surface

Ho-Chiao Chuang[a,*], Evan A. Salim[c], Vladan Vuletic[d], Dana Z. Anderson[c], Victor M. Bright[b]

[a] Department of Mechanical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan
[b] Department of Mechanical Engineering, University of Colorado, Boulder, CO 80309-0427, USA
[c] Department of Physics, University of Colorado, Boulder, CO 80309-0440, USA
[d] Department of Physics, and MIT Harvard Center for Ultracold Atoms, Massachusetts Institute of Technology, Cambridge, MA 02139-4307, USA

ARTICLE INFO

Article history:
Available online 18 January 2010

Keywords:
Atom chips
Bose–Einstein condensation (BEC)
Atom transistor
Atom tunneling
E-beam lithography
Suspended nanowires

ABSTRACT

This paper describes the design and fabrication of an atom chip to be used in ultra-high-vacuum cells for cold-atom tunneling experiments. A fabrication process was developed to pattern micrometer- and nanometer-scale copper wires onto a single chip. The wires, with fabricated widths down to 200 nm, can sustain current densities of more than 7.5×10^7 A/cm^2. Partially suspended wires, developed in order to reduce the Casimir–Polder force between atoms and surface, were also fabricated and tested. Extensive measurements for variable wire width show that the sustainable currents are sufficiently large to allow chip-based atom tunneling experiments. Such chips may allow the realization of an atom transistor.

1. Introduction

Atom-chip technology [1–9] has been developed rapidly over the last decade as a tool to control ultracold atoms. Micromachined supported and free-standing current-carrying wires on the atom chips have been used to create microscopic magnetic potentials for cooling, trapping, and transport of ultracold atoms. The atom-chip approach enables a variety of methods for manipulating cold atoms and obtaining a Bose–Einstein condensate (BEC) and related forms of ultracold matter. It mitigates the need for high-power, water-cooled magnetic coils and large power supplies. Typically when producing a BEC in a chip-based magnetic trap less than 5 W of power is dissipated by the chip, with current densities up to 10^8 A/cm^2. Under normal conditions this produces a trap with average trap frequencies of more than 1 kHz and a trap depth of more than 1 mK. The tight traps that can be achieved with atom chips allow for fast evaporative cooling of the atoms, which can lead to higher bandwidths for ultracold-atom sensors, and relaxes vacuum requirements.

Atom chips offer the prospect of integrated cold-atom circuits capable of complex functionality. They can be constructed from elementary building blocks as is done in microelectronics, and they may prove useful in fundamental physics research, precision scientific measurements, and quantum information technology [10–15]. A basic component of a conventional electronic circuit is the transistor. Cold-atom transistors have been proposed and theoretically investigated [16,17]. The simplest atom transistor utilizes a three-well potential in which quantum mechanical tunneling between "source" and "drain" wells is controlled by the number of atoms in the central "gate" well as shown in Fig. 1. When the number of atoms in the middle well is small, atom tunneling from the left into the right well is negligible (Fig. 2(a)). This is due to mismatched chemical potential between the middle well and the two other wells (Fig. 2(c)). Adding atoms to the middle well increases the chemical potential due to inter-atomic interactions (Fig. 2(d)) and enables tunneling of atoms from the left to the right well [16]. With appropriate choice of the potential, it is possible to control a large atom flux with a small number of atoms: behavior similar to that of an electronic transistor with current gain.

In order to achieve adequate tunneling rates in the device, the potential minima of the three wells should be as close together as possible; in the order of 1 μm or less. Ideally the sub-micrometer wires used to control atoms are suspended above the chip surface to mitigate the deleterious effects of atom-surface interactions [18]. Incorporating large current-carrying wires on the same substrate as sub-micrometer suspended wires presents a variety of technical challenges. The combination of electron-beam lithography and silicon micromachining techniques enables the fabrication of mechanical structures on the sub-micrometer scale. In this paper, we present a combination of techniques to demonstrate a chip capable of performing two-well atom tunneling experiments, with an eye towards more complicated structures that would enable the realization of an atom transistor. The details of

* Corresponding author. Tel.: +886 2 2771 2171x2076; fax: +886 2 2731 7191.
E-mail address: hchuang@ntut.edu.tw (H.-C. Chuang).

0924-4247/$ – see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2010.01.003

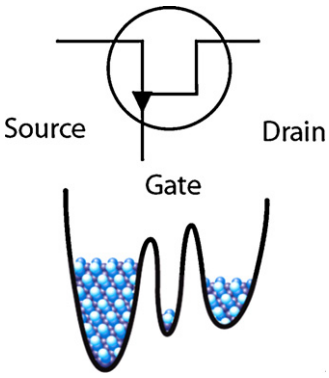

Fig. 1. The schematic drawing of an atom transistor.

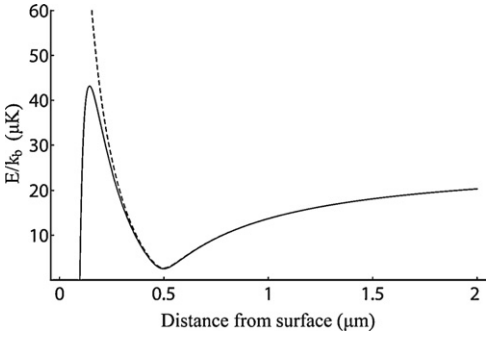

Fig. 3. Plot of the effects of the Casimir–Polder potential on the magnetic trap. Shown are the potentials for the nanowires directly on the surface (solid) and for the wires suspended 2 μm above the surface (dashed).

the design and fabrication process are described in the following sections.

2. Design of the atom transistor chip (theory and simulations)

The intended experiments rely on quantum mechanical tunneling of atoms between adjacent potential energy wells formed by magnetic fields. The potential must be designed to have tunneling rates that are large compared to the inverse lifetime of the atoms, which is about 100 ms when the atoms are within a few hundred nanometers of the chip surface [18], and the tunneling rate should not depend too sensitively on the well depth or atomic energy. The tunneling rate between wells can be estimated using a simple WKB calculation [19], which tells us that to satisfy the above conditions, the traps should be separated by not more than 1 μm. In order for the trap to have features of that scale, the trap has to be formed within the same distance of the wires, and the wire features must be below 1 μm. Unfortunately, fundamental problems arise when the atoms are placed so close to the surface: the attractive Casimir–Polder force between the atoms and the substrate will overpower the potential generated by the chip wires, and the atoms will crash into the surface. To mitigate this effect, we plan to use 100–500 nm wide wires suspended a few micrometers above the chip substrate. The primary loss mechanism of atoms due to the Casmir–Polder attraction will be tunneling of atoms through the magnetic potential into the chip surface. Since both the Casimir potential and the tunneling rate are extremely strong functions of distance a very small relief will be sufficient to make the surface interaction negligible. We estimate that a 2 μm relief should be adequate, which is consistent with the results of Ref. [18]. Fig. 3 shows the potential that the atom experiences for the case of the wire directly on the surface (solid) and when suspended 2 μm above the substrate (dashed). The Casimir–Polder potential is calculated using the method described in Ref. [20]. By placing several of these suspended wires in close proximity, it is possible to form multiple-well potentials with non-negligible tunneling rate (Fig. 4).

The nano-bridge wires confine the atoms tightly perpendicular to the direction of the nanowires. To generate a weak confinement in the other direction, we embed three wires into the silicon several micrometers beneath the nano-bridges as shown in Fig. 4(a). The three wires allow the trap to be operated in either the H-trap [21] or the dimple trap [22] configuration.

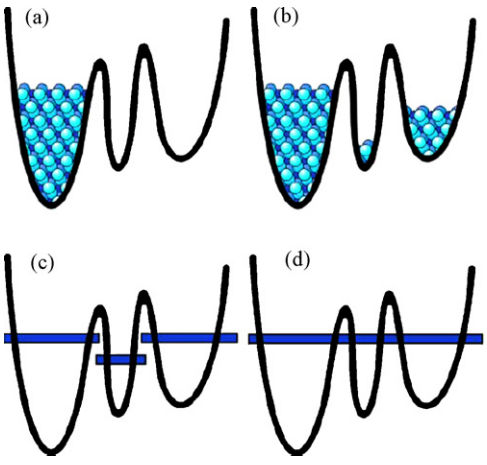

Fig. 2. The atom transistor uses a Bose–Einstein condensate in a triple-well potential.

3. Fabrication of the atom transistor chip

The atom transistor chip (Fig. 5) is created by a multi-layer metallization process with sacrificial oxide layers. The chip is made from a p-type double-side polished, 3 in. diameter silicon wafer (100 cut, 380 μm thick). A 300 nm thick silicon dioxide layer (SiO_2) was grown on both sides of the wafer as an insulating layer. Silicon etch windows on the oxide layer are patterned by HF (48%) for 15 s. A positive photoresist (AZ 4620) was then spin coated on one side of the substrate. After spinning, the wafer was baked on a hotplate for 5 min at 110 °C. After baking, the final thickness of the photoresist is around 6.5 μm. The three silicon trench etch windows (3 μm wide) are then patterned. The lithography is done with a mercury light source with a wavelength of 365 nm. The exposure time is 70 s and the developing time is 2.5 min in a dilute developer (1 part of AZ400K and 3 parts of DI water) at room temperature. The silicon trenches (2 μm deep) were etched by reactive ion etching (RIE). After the RIE etching, the photoresist was kept on the substrate for the self-alignment of the next two process steps: oxide sputtering and copper deposition. In order to have an insulating layer inside the silicon trenches, 100 nm oxide was sputtered inside the trenches. An adhesion layer, chromium (30 nm), and the bottom three copper wires (2 μm) were evaporated to fill up the silicon trenches. After metal evaporation, a lift-off process was performed to remove the metal layer from the surface of the substrate, except for the three embedded copper wires. A sacrificial oxide layer (3 μm) was sputtered on the top of the substrate. After oxide sputtering, the surface of the sputtered oxide was found not to be flat due to the three embedded copper wires underneath. Therefore, a chemical mechanical polishing (CMP) process was utilized to planarize the sputtered oxide surface as shown in Fig. 6(a) and (b). After the planarization, 1 μm of the sputtered oxide was removed. The photoresist used for electron-beam lithog-