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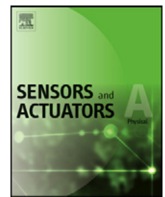

Pirani pressure sensor for smart wafer-level packaging

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ABSTRACT

Systems in Package (SiP) contain an increasing number of MEMS components such as resonators for time references or RF filtering. These resonators are packaged at wafer level and the cavity quality has to be guaranteed in terms of pressure and moisture level by the final manufacturing test. Therefore, environmental sensors could be integrated in the cavity to monitor these parameters and/or to calibrate the MEMS resonator with an electronic loopback. This paper presents the design of a low-cost Pirani pressure sensor for such application. First, the sensor principle is explained together with the fabrication process. Then, the closed-loop conditioning circuit, used to keep the sensor temperature constant, is described. It has been implemented on a first prototype that demonstrates a pressure measurement range extending over three decades, from 0.2 to 200 mbar. This range matches the cavity pressure level reached by some vacuum packaging techniques. In the end, the experimental results are used to develop a behavioral Matlab/Simulink model of the closed-loop sensor. This model provides simulation results in very good agreement with the experimental ones and it could be used to optimize the sensor design to cover an extended measurement range.

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1. Introduction

For mobile communications, radio frequency (RF) Systems in Package (SiP) are commonly used. Fig. 1 presents a SiP example from NXP Semiconductors where RF, analog, mixed signal and digital circuits are connected together by means of a silicon-based passive substrate. This substrate replaces the printed circuit board (PCB) and can be used to integrate RF passive components such as resistors or 3D-capacitors.

More recently, MEMS components have also been integrated within SiP. They need to be enclosed in a sealed cavity, the quality of which has to be guaranteed in terms of pressure and humidity. For this purpose, environmental sensors (temperature, pressure and humidity sensors) may be integrated in the wafer-level packaging so that the final manufacturing test consists in checking the environmental parameters directly from those sensors. Moreover, during the life of the system, a periodic check of these sensors may be useful to be sure that the MEMS performances are still within the specifications. At last, for a low deviation of the environmental parameters, and thus of the system performances, sensor data could be used to calibrate the functional MEMS using an electronic loopback. In this case, this smart wafer-level packaging will increase the manufacturing yield and the long-term stability of the system.

Monitoring the pressure level inside the cavity is particularly important for MEMS resonator packaged under vacuum conditions. Pressure directly impacts the quality factor of such structures. Typical vacuum level can range from 20 mbar down to 1 μbar, using a getter material inside the package [1,2].

This paper presents the design of a pressure sensor for such application. It is based on the Pirani gauge principle [3]: the pressure-dependent heat losses of a self-heated microbridge through a surrounding gas. First, the sensing principle and the fabrication technology are presented. Then, the conditioning circuit and the experimental measurements are shown. In the last part, a Matlab/Simulink model is described. Simulations are compared to the experimental results and some sensor improvements are proposed.

2. Sensor principle and fabrication

To reduce the cost we have chosen to integrate the pressure sensor in the passive RF substrate without any process modification (Fig. 1). It means that all the layer properties – thicknesses, doping, minimum width, overlaps, Young modulus, thermal conductivities, etc. – are set by the foundry for the RF SiP applications and cannot

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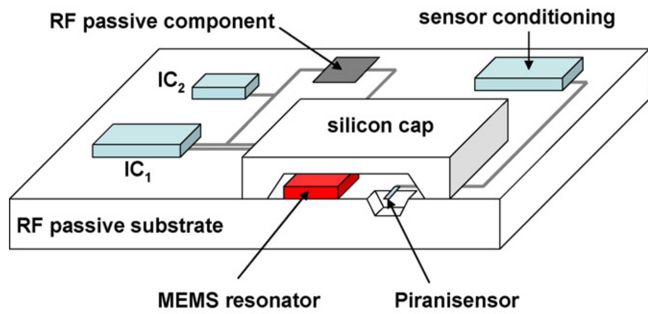


Fig. 1. SiP example with a cross section of a MEMS resonator packaged at wafer level.

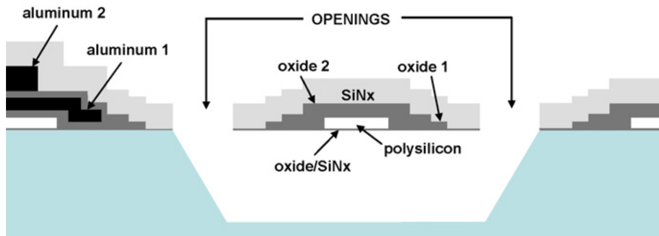


Fig. 2. Cross section of a FSBM-etched RF substrate.

be considered as design parameters for the MEMS designer. Fig. 2 presents a simplified cross section of this RF silicon substrate from NXP Semiconductors. First, silicon substrate is coated by a thin oxide/nitride layer of 50 nm. For MEMS manufacturing, a polysilicon layer, which is a good candidate for thermal or piezoresistive detection, and two aluminum layers are also available. Their thicknesses are 0.8, 1 and 3 μm, respectively. Two oxides and one nitride layers are also present for dielectric and passivation purposes. Their thicknesses are 0.3, 0.5 and 1.5 μm, respectively. Because this technology is not planar, front side bulk micromachining (FSBM) is possible without any process modification. This self-aligned post-process uses both via and contact openings to remove the dielectric layers and to define the etching mask [4]. Anisotropic silicon wet etching is then used to remove the silicon substrate underneath and to release micromechanical structures. The MEMS designer is able to freely define the size and shape of both cavities and suspended structures. It is also possible to choose the material implemented in suspended structures among the available materials – nitride, oxide, aluminum, polysilicon.

The post-process FSBM etching step is performed using a dual-doped TMAH solution. The critical issue of the etching is the selectivity. Both aluminum and dielectric etch rates must be as low as possible to obtain a well-defined cavity without degradation of the suspended structures. The etching solution preserves aluminum as long as some additives are mixed together with TMAH: dissolved silicon (Dis. Si) or silicic acid (SiAc) and an oxidation agent like ammonium persulfate (AP). Reported $Si_{\langle 100\rangle}$, Al and SiO_2 etching rates of TMAH solutions are presented on Table 1 [5–7]. These results seem to show that a 5% TMAH solution with doping concentrations higher than 30 and 5 g/l, for SiAc and AP, respectively,

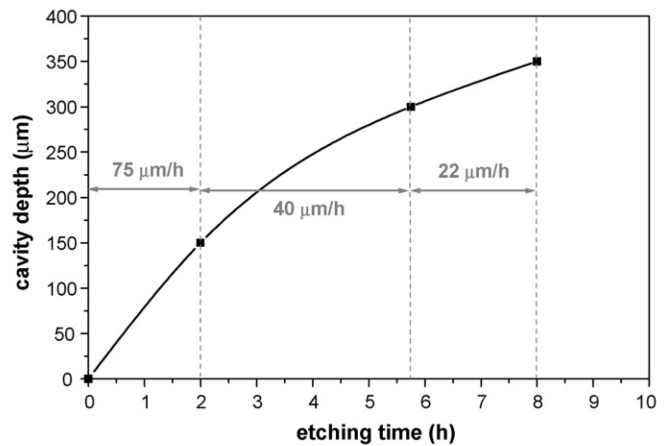
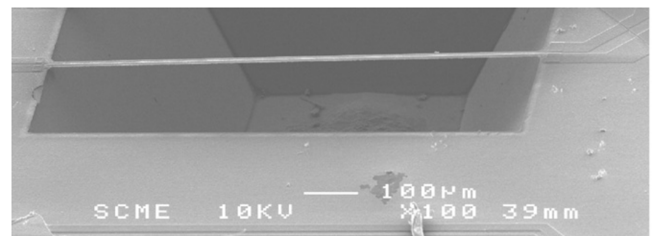


Fig. 3. Variation of the $Si_{\langle 100\rangle}$ etching rate.



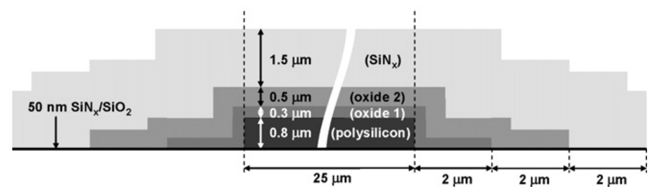


Fig. 4. SEM image and cross section of the beam.

should be enough for silicon etching at 80 °C with a good selectivity.

The preparation of our TMAH dual-doped solution is as follows: 50 g of pentahydrated TMAH (99% purity) is dissolved in 475 ml of de-ionized water to obtain a 5% TMAH solution in weight. This solution is heated up to 50 °C before 18 g of SiAc is added. The solution is stirred to allow the complete dissolution of the SiAc. The solution is then heated up to 80 °C (the etching temperature) and few minutes before the use, 3.5 g of AP are added. At this point, the die is immersed and the etching starts. Note that such TMAH dual-doped solutions are known to age rapidly [7]. Fig. 3 presents the cavity depth according to the etching time. At the beginning, the average $Si_{\langle 100\rangle}$ etching rate is 75 μm/h but it decreases to 22 μm/h after a few hours. For this reason, the non-released structures are transferred to a fresh solution after 8 h of etching.

Fig. 4 shows a SEM image of the bridge and its cross section. A small angle with respect to the wafer orientation permits to release it in 1 or 2 h but longer etching times allow deeper cavities. Its

Table 1
$Si_{\langle 100\rangle}$, Al and SiO_2 etching rates.

TMAH	R_{Si} (μm/h)	R_{Al} (nm/h)	R_{SiO_2} (nm/h)	Refs.
3%, 80 °C	60	36000	180	[3]
2%, 80 °C, dual-doped: SiAc (30 g/l) and AP (5 g/l)	85	3.5	0.7	[3]
5%, 80 °C, dual-doped: SiAc (38 g/l) and AP (7 g/l)	70	4.5	0.7	[3]
5%, 85 °C, Dis. Si (1.6 wt.%) and AP (>0.5 wt.%)	55	≈0	<1	[4]
5%, 80 °C, dual-doped SiAc (20 g/l) and AP (6 g/l)	35	–	–	[5]

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