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An integrated energy-efficient capacitive sensor digital interface circuit

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ABSTRACT

In this paper, we propose an energy-efficient 13-bit capacitive sensor interface circuit. The proposed design fully relies on successive approximation algorithm, which eliminates the need for oversampling and digital decimation filtering, and thus low-power consumption is achieved. The proposed architecture employs a charge amplifier stage to achieve parasitic insensitive operation and fine absolute resolution. Moreover, the output code is not affected by offset voltages or charge injection. The successive approximation algorithm is implemented in the capacitance-domain using a coarse-fine programmable capacitor array, which allows digitizing wide capacitance range in compact area. Analysis for the maximum achievable resolution due to mismatch is provided. The proposed design is insensitive to any reference voltage or current which translates to low temperature sensitivity. The operation of a prototype fabricated in a standard CMOS technology is experimentally verified using both on-chip and off-chip capacitive sensors. Compared to similar prior work, the fabricated prototype achieves and excellent energy efficiency of 34 pJ/step.

1. Introduction

Capacitive sensors find numerous applications in the consumer, medical, automotive, and industrial sectors [1]. The range of applications includes, but is not limited to, pressure sensors [2,3], humidity sensors [4], tactile sensors [5], biological sensing microsystems [6], and chemical detection of volatile organic compounds (VOCs) [7] which can be used as biomarkers for early non-invasive detection of lung cancer [8]. Although the type of application imposes different performance requirements on the sensor interface circuit, energy efficiency is always desirable.

Recent trends in capacitive sensing interface circuits favor direct digitization of the sensor capacitance, rather than performing capacitance to voltage conversion and then digitizing the output voltage [9–12]. Direct digitization offers less complexity, smaller area, and lower power consumption [9–12]. In a "semi-digital" approach, the capacitance can be used to modulate the period or the pulse width of a digital signal [9,12]. However, this approach requires a time-to-digital converter in order to provide digital output code, e.g., a fast digital counter and a stable high frequency oscillator [12], which hinders its use in a low-power application. A more attractive approach for capacitance-to-digital conversion (CDC) is the use of $\Delta\Sigma$ modulators [10,11,13]. However, oversampling and digital decimation filtering required in $\Delta\Sigma$ architectures translate to large power consumption. In addition, $\Delta\Sigma$ interfaces suffer from limited capacitance range to avoid modulator overload [10,11]. In order to increase the capacitance range of $\Delta\Sigma$ interface circuits, successive approximation register (SAR) algorithm was proposed to adjust the modulator reference capacitor [10,11]. However, the SAR step was only used for initial coarse calibration, while sensor digitization is still performed using the $\Delta\Sigma$ modulator.

A capacitance-to-digital converter (CDC) architecture that fully relies on SAR algorithm will eliminate the need for oversampling, which will reduce power consumption and relax the requirements on the analog blocks. Moreover, digital output code is directly provided with no digital filtering required, which further reduces power consumption. A CDC that fully relies on SAR algorithm was proposed in [14], using an op-amp-less architecture. However, due to the absence of the op-amp, the sensor capacitance is connected to a high impedance node which leads to parasitic sensitive design. Moreover, as no charge amplifier stage is present, the change in voltage (ΔV) that needs to be resolved by the comparator will be inversely proportional to the total sum of the capacitances of the parasitic capacitors, the capacitive sensor, and the SAR capacitor array, which will result in poor absolute resolution (more than 60 fF for the design in [14]), in addition to sensitivity to noise, charge injection, and offset voltage. When the CDC circuit is connected to off-chip capacitive sensor, the parasitic capacitor can be very large

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leading to degradation of the circuit performance. Furthermore, connecting the CDC circuit to off-chip capacitive sensor using a high impedance node makes it highly susceptible to noise coupling.

In this work, an integrated 13-bit SAR CDC that addresses the previous limitations while maintaining excellent energy efficiency is presented. The proposed CDC employs a charge amplifier stage, which results in insensitivity to parasitic capacitors, insensitivity to charge injection and offset voltages, fine absolute resolution, and immunity to noise coupling. The SAR algorithm is performed in the capacitance-domain using a coarse-fine programmable capacitor array (PCA), which enables digitizing a wide range of capacitance in a compact area. The proposed CDC is insensitive to the value of any reference voltage or current, which translates to very small temperature sensitivity. As the circuit operation is insensitive to parasitic capacitances, it can be used robustly with on-chip and off-chip capacitive sensors and multiplexed capacitive sensor arrays.

The proposed SAR CDC is implemented in a 0.35 μm standard CMOS technology. The prototype is capable of digitizing 16 pF capacitance range with 2.75 fF resolution, while occupying only 0.07 mm^2 of the chip area. The operation of the fabricated prototype was experimentally verified by using both on-chip and off-chip capacitive sensors. The achieved energy efficiency is 34 pJ/step which is better than recently published capacitance-to-time and $\Delta\Sigma$ CDCs that are implemented using the same technology and supply voltage [10,12], which shows the merit of the proposed architecture.

The rest of the paper is organized as follows. The operation of the proposed circuit is discussed in Section 2, in addition to analysis of the circuit nonidealities. Section 3 describes the programmable capacitor array (PCA). The limits of the PCA resolution and dynamic range due to mismatch are analyzed and calculated. System description and the operation of the digital interface are given in Section 4. Experimental results of the fabricated prototype are presented in Section 5.

2. Successive approximation CDC

2.1. Circuit operation

The schematic of the proposed SAR CDC circuit is shown in Fig. 1. C_{SENS} is the unknown capacitive sensor and C_{REF} is a reference capacitor implemented as a binary weighted programmable capacitor array (PCA). $U1$ is a two-stage Miller compensated op-amp with a PMOS input unbalanced differential pair and $U2$ is a comparator. The circuit operation is divided into two phases; the precharge phase and the evaluate phase. During the precharge phase ($CLK = 1$, $CLKB = 0$), the op-amp ($U1$) is working as a unity gain buffer, i.e., $V_X = V_{REF}$. The charge on the sensing capacitor (C_{SENS}) is given by

$$Q = C_{SENS} \times V_{REF} \tag{1}$$

Next, in the evaluate phase ($CLK = 0, CLKB = 1$), the voltage difference across C_{SENS} is zero, and the charge redistributes to the reference capacitor (C_{REF}) and the feedback capacitor (C_F). The charge is given by

$$Q = C_{REF} \times V_{REF} + (V_{REF} - V_o) \times C_F \tag{2}$$

As the charge is conserved, from (1) and (2), the output of the op-amp is given by

$$V_o = V_{REF} + V_{REF} \times \left(\frac{C_{REF} - C_{SENS}}{C_F}\right). \tag{3}$$

Thus, the differential input of the comparator (U2) is given by

$$\Delta V_o = V_o - V_{REF} = V_{REF} \times \left(\frac{C_{REF} - C_{SENS}}{C_F}\right),$$

and the output of the comparator is given by

$$V_{CMP} = \begin{cases} 0, & \Delta V_o > 0 \\ 1, & \Delta V_o < 0 \end{cases} = \begin{cases} 0, & C_{REF} > C_{SENS} \\ 1, & C_{REF} < C_{SENS} \end{cases}. \tag{4}$$

Based on V_{CMP}, the SAR logic changes the PCA digital input to increase or decrease C_{REF}, using a binary search successive approximation algorithm. The logic was implemented off-chip for testing flexibility. At the end of the conversion cycle, the value of C_{REF} is matched to C_{SENS} within an error of 1LSB of the PCA. The conversion time is $N \times T_{CLK}$, where N is the number of bits of the PCA and T_{CLK} is the period of the conversion clock (CLK). The value of V_{REF} is set to 1.45 V which is roughly at the middle of the common-mode input-range of both the op-amp and the comparator. However, the circuit operation is insensitive to the value of V_{REF}. Any variation or drift in V_{REF} will equally affect both $U1$ and $U2$, and thus it will be canceled and (4) will remain valid. The digital output of the comparator is determined by the sign of ΔV_o regardless of its absolute value. Any drift or variation in V_{REF} will change the absolute value of ΔV_o but it will not change its sign, because the sign is determined by the difference ($C_{REF} - C_{SENS}$). Thus, variation in V_{REF} will not affect the circuit functionality because it will not change the output of the comparator.

For a SAR ADC, only one active block (a comparator) is required, as the input signal is a buffered analog voltage. However, for a SAR CDC which directly converts capacitance to digital output, an

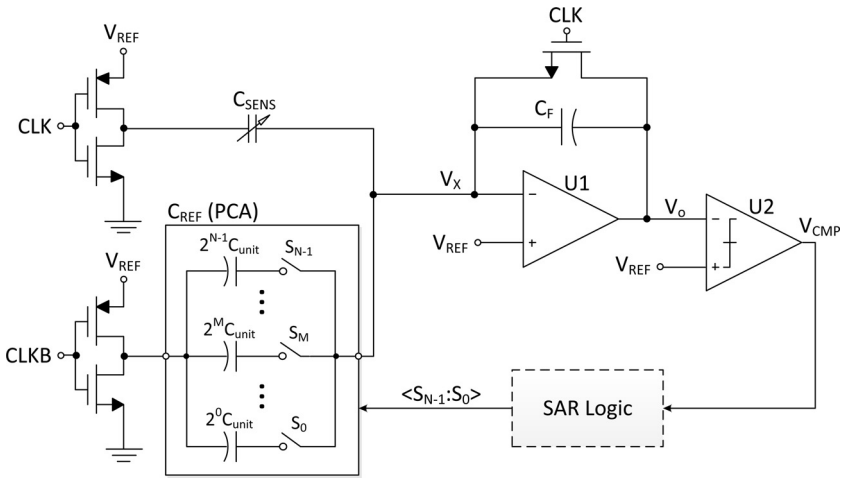

Fig. 1. Schematic of the proposed SAR CDC circuit.