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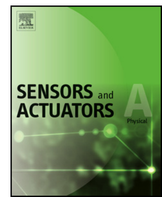

Highly insulating, fully porous silicon substrates for high temperature micro-hotplates

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ABSTRACT

As alternative to established thermal substrates and thin membranes, we have investigated fully porous silicon substrates as highly insulating material for thermal devices. Exhibiting a thermal conductivity similar to silica glass and considerably lower than silicon nitride due to increased phonon scattering, thick mesoporous silicon also offers improved thermal and mechanical stability. Our work has focused on full wafer thickness porosification as a not extensively documented use of porous silicon and its application to thermal devices. Here we present measurement and finite element simulation results for our latest generation thin film microheaters on fully porous silicon substrates as proof of concept devices. Porosity, mass density, and specific heat capacity of porous silicon are deduced from fabrication parameters, thermal conductivity is determined by the so-called 3ω-measurement method, and all material properties are validated by fitting measurement data to our finite element models. For thick fully porous domains we estimated a thermal conductivity of ≈0.9 W/m/K, as well as a density of ≈1200 kg/m^3, a specific heat capacity of ≈780 J/kg/K and a corresponding volumetric porosity of ≈50%. Thin film fabrication of nitride passivation and molybdenum meander microheaters on fully porous domains allowed characterization of thermal performance and insulation. For 10 mm^2 microheaters we measured a power efficiency of 0.40 K/mW stable up to a maximum temperature of 475 °C, compared to 0.37 K/mW stable up to 440 °C on silica glass. Both static and dynamic heater measurements show superior performance of fully porous silicon substrates compared to reference samples on thin silica glass substrates.

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1. Introduction

Thermal effects are used for a wide range of sensors and actuators in microsystems, with miniaturization offering, e.g., improved sensitivity, decreased reaction times, reduced energy consumption, and easier integration with other microsystem components. Highly localized temperature hotspots, large temperature gradients, precise spatial and temporal temperature and heat flow control can be achieved to realize temperature sensors, flow sensors, microheaters, or gas and humidity sensors. In order to facilitate such precise control, thermal insulation between regions of different temperatures to minimize thermal losses poses one of the biggest challenges in design and fabrication of such devices. One standard approach is to place the heated structures onto thin, often suspended membranes made of materials with low thermal conductivity, e.g. silicon nitride membranes, thin glass substrates, or more exotic material combinations [1–3]. A disadvantage to this approach is the increasing fragility and decreasing stability of thinner and thinner membranes or substrates of a few microns down to a few 10 nm.

In our work we have been investigating alternative technologies for improved performance of thermal devices. One such technology is the use of porous silicon as membrane or substrate material. Porous silicon (pSi) is a rather new material with unique physical properties and compatible to standard MEMS processing technologies [4–6] developed for use in a variety of applications, ranging from, e.g., optical and photonic devices [7,8], bulk sacrificial and structural material for MEMS [9–13], microfluidic devices [14,15], gas sensors [16,17], explosives [18], to thermal insulation layers [19]. Porous silicon can be electrochemically etched from bulk silicon wafers. The remaining silicon crystallites retain high mechanical stability, however at pore sizes below the mean free path of thermal phonons [20] and depending on porosity and pore morphology, the thermal conductivity is drastically reduced to the same order of magnitude as silica glass and below that of silicon nitride [21–23]. While a number of applications utilizing mesoporous silicon insulation layers and membranes of up to several 10 μm thickness have been demonstrated [24–26], to our

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knowledge fully porosified substrates have been attempted [27], but have not yet been extensively characterized and applied to thermal devices. As presented in this paper, moderately thick porous silicon substrates offer a promising alternative to fragile membranes or substrates.

To verify our approach of fully porous silicon substrates, we have extensively characterized our porous silicon fabrication process in terms of achievable volumetric porosity, etch rate, as well as pore size and morphology [28]. We utilized the 3ω-method for thermal conductivity measurements on thick porous silicon layers. We deposited thin film molybdenum microheaters on porous silicon, as well as on reference silicon and silica glass substrates for static and dynamic micro-hotplate characterization. Measurement results for first generation samples already showed a notable improvement, as published previously [29], however not achieving thermal insulation similar to the glass reference due to a thin residual non-porous silicon slice in the center of the porous region acting as thermal shortcut. In the following chapters, we will present the latest results of an improved fabrication process with backside thickness reduction for our second generation samples with confirmed full thickness porosification yielding device characteristics similar to or even better than microheaters on glass substrates or membranes. Additionally, we developed simulation models using the finite elements method (FEM) to validate the material properties of the fully porous silicon substrates by comparison with measurement data and thermal imaging.

2. Thick, fully porous silicon substrates

Porosification of silicon is an electrochemical wet etching process utilizing hydrofluoric acid (HF) to locally anodize the wafer surface and etch pores into single-crystalline silicon substrates. Anodization is achieved by the accumulation of positive charges (holes) at the semiconductor surface due to the presence of an electric field, which remove covalent bonds of surface atoms to the bulk material and thus increase the susceptibility to dissolution or oxidization of these atoms in the HF electrolyte. Operating in a high anodic potential regime with a surplus of holes arriving at the silicon–electrolyte interface results in etching on the whole wafer surface, a process termed electropolishing of silicon. Conversely, operating in a low anodic potential regime by limiting the applied current and thus the amount of positive charges leads to a statistically distributed etching effect. Here, these initial etch pits and other defect sites offer preferential break-through locations for further charges, yielding pore growth into the depth of the substrate. A general review of pSi formation, properties, and applications can be found in, e.g., [4–6,30–32]. Resulting porosity, etch rate, and pore morphology are dependent on a wide variety of process parameters. For the application as thermal insulation layers, small pore sizes, high porosities and sponge-like pore morphology are most desirable. The fabrication setup, electrochemical etching process, characterization of fabrication parameters, as well as process challenges of our work have been published previously [29].

2.1. Porosity and morphology

Volumetric porosity P as the ratio between pores/air and remaining silicon can be estimated gravimetrically by $P = (m_0 - m_1)/(m_0 - m_2)$ where m_0 is the initial mass of the wafer, m_1 the mass after porosification, and m_2 the mass after removal of the porous silicon in a weak potassium hydroxide (KOH) solution. The obtained volumetric porosity for (100) p^+-type silicon wafers ranged from 20% to 85% with a standard deviation of 2.6% for repeated etch steps. The layer thickness d_{pSi} can also be calculated from gravimetric measurements by $d_{pSi} = (m_0 - m_2)/(\rho_{Si} \times A)$, where ρ_{Si} is the mass density of silicon and A the effective wafer surface area under etch. The average etch rate r is then calculated using the etching time, resulting in a range of a few micrometer per minute and up to 10 μm/min with a standard deviation of 3%. Aside from thickness verification we also used a surface profiler (*Dektak XT Stylus Profiler*, Bruker Nano) for etch profile determination. For most of the wafer surface the etch depth is uniform within ≈1%, however, there is a pronounced overetching of around +10% at electrically insulated edges of each etch region due to a converging electric field and therefore a local increase of the current density. When etching through a complete substrate this edge effect leads to a local “break through” spots with a large local current density increase resulting in large local mechanical stress. To reduce this stress effect we employ an alternated double-side etching scheme described in Section 2.3. The effective heat capacity of porous silicon as the product of mean mass density and specific heat capacity of the remaining silicon crystallites can be determined directly from the volumetric porosity.

Pore size and morphology, investigated via SEM imaging and documented in [29], show a mesoporous surface with pore sizes between 5 and 40 nm. For standard samples with 50–60% porosity we measured pore sizes of around 15 nm and the desired sponge-like morphology. Investigation of the breaking edge of a sample from the center region of a fully porosified wafer also indicated full wafer porosification with little to no remaining bulk silicon which could act as a thermal shortcut and reduce the insulation effect.

2.2. Thermal conductivity

To determine the thermal conductivity of these porous silicon substrates we employed the 3ω-measurement method [33]. Applying a sinusoidal heating current at frequency ω across a line source heater generates a thermal wave propagating into the substrate at 2ω, which results in a corresponding resistance modulation of the heater line. By virtue of Ohm’s law, this dynamic resistance modulation together with the driving current yields additional spectral voltage components at frequencies ω and 3ω. The amplitude of the 3ω component is only related to the temperature amplitude ΔT, i.e., $U_{3\omega} = 1/2\, \alpha R_0 \Delta T I_0$, with temperature coefficient α, operating resistance R_0, and driving current amplitude I_0 as parameters. The penetration depth of the thermal wave is determined by the square root of thermal diffusivity D divided by 2ω. Here, $D = \lambda/(\rho c_p)$, with thermal conductivity λ and ρc_p the volumetric heat capacity. Within the constraints of penetration depth smaller than layer thickness but much larger than width of the heater to satisfy the line source condition and with the limitation to isotropic and homogeneous materials, an approximate solution for the temperature amplitude has been established [33]. In complex notation assuming a harmonic time dependence $\exp(j\omega t)$, the temperature amplitude ΔT can be written as $\Delta T = P/(\pi l \lambda)\ [1/2 \ln(4D/r^2) - 1/2 \ln(2\omega) - \gamma + j\pi/4]$ with $\gamma \approx 0.5772$ being the Euler–Mascheroni constant and j the imaginary unit. The real part of the temperature change is proportional to the logarithm of the frequency, with parameters being heating power P per unit length l and thermal conductivity λ of the penetrated material. Therefore the slope of a $\mathrm{Re}(\Delta T) - \ln(\omega)$ plot taken from the measurement of the 3ω component of the voltage across a line source heater allows direct determination of the thermal conductivity.

We utilize a custom tunable measurement circuit with a Wheatstone bridge layout driven by an arbitrary function generator (*Agilent 81150A*), bridge output amplified by an instrumentation amplifier (*INA 129U*, Texas Instruments) and the 3ω component extracted with a lock-in amplifier (*SR830*, Stanford Research Systems). An exemplary measurement result is given in Fig. 1 for a 175 μm thick pSi layer on silicon substrate (red dots) compared to

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