Sensors and Actuators A 195 (2013) 160–166

Contents lists available at SciVerse ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

I-shaped thermally actuated VHF resonators with submicron components

H.J. Hall[a,*], A. Rahafrooz[b], J.J. Brown[a], V.M. Bright[a], S. Pourkamali[b]

[a] Department of Mechanical Engineering, University of Colorado at Boulder, Boulder, CO 80309-0427, USA
[b] Department of Electrical and Computer Engineering, University of Denver, Denver, CO 80210, USA

ARTICLE INFO

Article history:
Received 14 April 2012
Received in revised form 6 December 2012
Accepted 10 December 2012
Available online 20 December 2012

Keywords:
Resonator
Thermal actuator
Piezoresistive
VHF

ABSTRACT

Thermally actuated piezoresistive readout single crystal silicon (SCS) resonators with a device footprint of ~110 μm^2 have been experimentally demonstrated at operating frequencies of 112–176 MHz. An SOIMEMS fabrication process was developed which incorporates electron beam lithography to achieve submicron dimensions. Demonstrated performance under vacuum (50–70 Torr) includes a Q = 5750 and motional conductance of 89.6 μA/V. Frequency tunability of 2.1% in ambient and 3.66% under vacuum is achieved by variation of the DC bias current. The effects of asymmetry of the devices on operating frequency due to fabrication imperfections are considered qualitatively using commercial modeling software.

1. Introduction

The concept of thermally actuating high frequency resonators and utilizing piezoresistors to sense their motion has been around for a considerable amount of time [1,2] and continues to be used in designs today [3–5]. Operation of these devices is based upon modulation of local thermal gradients within the resonant structure to excite particular structural modes. This has been typically accomplished through localized Joule heating of resistors on the surface of the structure created by ion implantation. The approach is relatively simple in both fabrication and operation compared to traditional alternatives, which either require ceramic films (piezoelectrics) or nanoscale gap formation (capacitively driven and/or sensed devices).

Recently an alternative approach to thermal-piezoresistive resonant devices has been considered with the development of in-plane extensional mode resonators fabricated entirely by patterning a single layer of uniformly doped single-crystal silicon (SCS) [6–8]. The concept of operation is similar to the aforementioned devices except the localized regions in which the heating occurs are explicitly controlled through the geometry of the devices. In addition, for two-terminal operation, the piezoresistive readout is integrated into the device structure (i.e. no additional readout resistors are required). The merits to this approach are primarily two-fold: (1) the fabrication is simpler, as no additional patterning of resistors or doping is required, making aggressive size reduction possible and potential on-chip integration with electronics easier; and (2) if the piezoresistive coefficient of the material is negative and its small signal voltage to current gain, or motional conductance, is sufficiently high an phenomenon known as self-Q enhancement [9] can occur from internal positive feedback; this can allow device operation as a oscillator without the need for additional circuitry [10]. Thus there exists considerable potential for these devices in both sensing applications and on-chip RF electronics.

Previous work [6] has fabricated the I-shaped or dumbbell geometry (see Fig. 1) using a conventional SOIMEMS process and demonstrated frequencies up to 61 MHz with device footprints of 350 μm^2 or larger. While the performance of the previously reported devices was impressive (Q up to ~38,000; motional conductance up to ~25 mA/V) lumped element theory predicts that the performance should improve dramatically as critical dimensions are scaled to smaller sizes for higher operating frequencies [6]. In addition, as these devices could be potentially applied toward on-chip RF signal processing, further miniaturization affords the possibilities of denser integration and continued reduction of the footprint of analog electronics and integrated circuits. The central motivation for this work was to examine this premise experimentally and develop an understanding of the effects of reducing dimensions on device performance. This paper presents the initial work toward this effort, expanding upon the results reported in [11], using I-shaped resonators with submicron feature sizes fabricated from a thin SOI device layer.

2. Device operation and performance metrics

The operation of the thermal-piezoresistive resonant devices in this work primarily results from the interaction of the mechanical, thermal, and electrical response of the center actuator arms

* Corresponding author at: Department of Mechanical Engineering, University of Colorado - Boulder, 427 UCB, Boulder, CO 80309-0427, USA. Tel.: +1 3034927151.
E-mail address: Harris.Hall@colorado.edu (H.J. Hall).

0924-4247/$ – see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.sna.2012.12.006

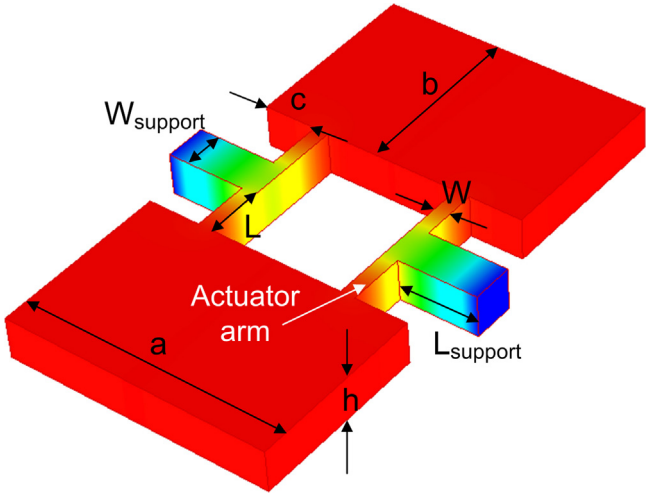

Fig. 1. Graphical schematic of I-shaped or dogbone resonator geometry with dimensions. Colors are indicative of an arbitrary steady state temperature distribution for DC applied voltage with the support anchor ends acting as heat sinks at a fixed temperature. The temperature gradient evident in the actuator arms (width = W, length = L) is amplitude modulated by the addition of an AC drive voltage. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

in the structure (indicated in Fig. 1). Like all thermally actuated resonators, due to the square relationship between ohmic power loss and electrical voltage, a combination of AC signal and DC bias voltages is required for a frequency component of the cyclic Joule heating to match that of the applied AC signal. Excitation with AC voltage alone is possible, but the resonant mechanical response would occur at a frequency twice that of the input voltage. The alternating tensile and compressive stresses from thermal expansion and contraction of the actuator arms is sufficient to induce excitation, despite the cutoff frequency of the thermal response of the actuator typically being much less than the intrinsic mechanical frequency of the structure's longitudinal mode. When the material exhibits significant piezoresistivity, this expansion/contraction of the arms causes modulation of the DC current, leading to an AC current component called the motional current, which can be detected. In this geometry, because the longitudinal acoustic waves which propagate from the actuator arms are perpendicular to the support arm the amount of leakage through the support arms is reduced in comparison to geometries where the actuator also acts as a structural support to the substrate [7,8,12].

By considering the electrical, thermal, and mechanical subsystems, lumped systems analysis of the device dynamics [6], yields the small signal voltage to current gain, or motional conductance, g_m, to be:

$$g_m = 2\alpha E \pi_l Q \frac{I_{dc}^2}{C_{th}\omega_o} = 2\alpha E \pi_l \frac{I_{dc}^2}{C_{th}\Delta\omega} \quad (1)$$

where α is the coefficient of thermal expansion, E is Young's modulus (130×10^{11} Pa for ⟨1 0 0⟩ silicon), π_l is longitudinal piezoresistive coefficient modulus ($\sim 50 \times 10^{-11}$ Pa^{-1} for ⟨1 0 0⟩ silicon as suggested by [13]), Q is the quality factor, I_{dc} is the dc current, C_{th} is the thermal capacitance of a pair of actuator arms, ω_o is the natural undamped mechanical resonant frequency, and $\Delta\omega$ is the full width half maximum (*FWHM*) of the resonant peak. In this formulation the mechanical system is considered a classic driven harmonic oscillator (2nd order mass-spring-damper). The geometric dimensions and the elastic modulus of the material in turn define the natural mechanical resonant frequency of the extensional (or longitudinal) mode of the structure. The dampening inherent to the resonator is captured by either Q or *FWHM*. Optimum device performance entails both maximizing the motional conductance and minimizing the power consumption. To capture both of these factors a figure of merit (FOM) which ratios the two is defined as

$$\text{FOM} = \frac{g_m}{P_{dc}} = \frac{2\alpha E \pi_l Q}{C_{th}\omega_o(R_A + R_S)} \quad (2)$$

where P_{dc} is the DC power, R_A is the resistance of the actuator arm, and R_S is the additional series resistance of the resonator. Per (1) and (2) if the device is scaled down by a factor S, g_m increases by a square relationship (i.e. g_m is proportional to S^2), and FOM increases linearly (i.e. FOM is proportional to S).

The driving factor in the improvement with scaling lies with the thermal capacitance of the actuators' arms. A single pair of actuator arms can be considered to have an effective thermal capacitance, C_{th}, of

$$C_{th} = \beta C_{LE} = 2\beta\rho LWhc_H \quad (3)$$

where C_{LE} is the lumped-element thermal capacitance, β is a correction factor which has been established from finite-element analysis [14] to be between 1.02 and 1.11, ρ is the density (2.33×10^{-15} kg/μm^3 for silicon), W is the actuator width, L is the actuator length, and c_H is the specific heat of silicon (700 J kg^{-1} K^{-1}). The factor of 2 is included because this capacitance represents a pair of individual actuators as defined in Fig. 1.

3. Device fabrication

The fabrication process, shown in Fig. 2, was adapted from previous work to accommodate electron beam lithography (EBL) and subsequent patterning of necessary submicron critical device dimensions. The starting wafer was silicon-on-insulator (SOI) with a 340 nm Si (1 0 0) device layer and 1 μm thick buried oxide (BOX) layer on a conductive silicon substrate. Originally doped p-type with boron (14–22 Ω-cm per the manufacturer), the device layer was compensation doped to n-type with phosphorus. Device patterning was performed along the ⟨1 0 0⟩ direction to maximize the negative amplitude of the longitudinal piezoresistive coefficient, π_L. Resistivity of the device layer was measured by 4-point probe to be ~0.01 Ω cm. The two-terminal device interconnect pads (area ~145,000 μm^2 each) and alignment markers were patterned from a thermally evaporated 100 nm Cr/25 nm Au metal stack using photolithography (S1813 photoresist) and lift-off. The metal pads were linked by a 14 μm × 20 μm rectangular bridge from which the devices were patterned. The Au layer was needed only to provide necessary visibility of the EBL alignment markers and was removed from a 30 μm square area centered about the bridge using photolithography and wet etching (Transene TFA Au Etchant). Patterning of the device geometry was then performed using EBL (JEOL JSM-5910LV SEM with Nanoscale Pattern Generation System software) of PMMA and developed. The pattern was transferred to the Cr using a timed wet etch (Cyantek CR-7S). Reactive Ion Etching (RIE) was performed (5 sccm SF_6: 15 sccm CHF_3, 150 W, 10 mTorr) to etch the device pattern into the silicon device layer. After the silicon etch the remaining Au and Cr were stripped in wet etchants and rinsed in deionized water. Since the BOX acts as an etch stop for this RIE chemistry, profilometry scans (Dektak 3030) were performed on the pads to check the device layer thickness after metal stripping. Device layer thickness was confirmed to be 340 ± 10 nm. To complete fabrication, the devices were released in 48% $HF_{(aq)}$ (4 min etch time) followed by CO_2 critical point drying (Fig. 3).

Close examination of the devices using scanning electron microscopy showed that the etching was anisotropic with ~15° of outward slope. In addition, significant roughness along the edges and filleting of the corners was apparent. Seven measurements were performed across the top surface for each dimension of the