Sensors and Actuators A 181 (2012) 77–80

Contents lists available at SciVerse ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

RF-MEMS switch with through-silicon via by the molten solder ejection method

Shinpei Ogawa*, Shinnosuke Soda, Sang-Seok Lee[1], Shinichi Izuo, Yukihisa Yoshida

Advanced Technology R&D Center, Mitsubishi Electric Corporation, 8-1-1 Tsukaguchi-Honmachi, Amagasaki, Hyogo 661-8661, Japan

ARTICLE INFO

Article history:
Received 26 December 2011
Received in revised form 2 March 2012
Accepted 18 April 2012
Available online 25 April 2012

Keywords:
RF-MEMS switch
TSV
Packaging
Molten solder

ABSTRACT

A radio frequency-microelectromechanical system (RF-MEMS) switch with through-silicon via (TSV) technology for hermetic packaging was designed and developed using the molten solder ejection method (MSEM). High frequency simulation was used to determine the lowest loss of the shift-aligned ground-signal-ground (GSG) TSV structure. The RF-MEMS with shift-aligned TSV was successfully developed by integrating surface micromachining with MSEM. The electrical properties of RF-MEMS switches with the shift-aligned TSV were measured, and a low insertion loss of 0.1 dB at 15 GHz was achieved for a GSG TSV configuration.

1. Introduction

Radio frequency-microelectromechanical system (RF-MEMS) switches possess significant advantages over PIN diode or field-effect transistor (FET) switches, such as near-zero power consumption, high isolation, and low insertion loss. Many applications are being developed that can employ RF-MEMS switches, such as reconfigurable antennas and tunable band-pass filters [1,2]; however, RF-MEMS switches require hermetic packaging to protect their contacts from contamination and the electrical interconnection between the packaged MEMS device and external circuits. Therefore, the interconnection is crucially important to maximize the potential for RF-MEMS device performance [3].

Two approaches to the interconnection can be defined: a buried feedthrough with a planar signal line structure and through-silicon via (TSV) with a vertical connection. Although buried feedthroughs have the advantage to utilize conventional planar silicon processes, disturbance of the feedthroughs by the seal ring causes degradation of the high frequency performance. There has been increasing interest to address this issue in TSV and various methods are being developed, such as Cu electroplating [4–6], bottom-up Cu electroplating [7] and filling with molten solder [8]. Cu has an advantage as the filling material with respect to resistivity. However, the difference in transmission loss between Cu and solder is negligible in the short pass of TSV, because of the skin depth effect in the high frequency region. TSV has an advantage for RF and millimeter-wave applications, due to its shorter pass and minimum inductance. It also matches with both the surface mounting technology and vertical 3D chip stacking technology, which results in high density device packaging. On the other hand, there are still difficulties in TSV technology, such as the complicated fabrication process, achieving hermeticity, high power handling, and the electrical design for high frequency operation.

TSV by the molten solder ejection method (MSEM) [9] is proposed in this study for the high frequency interconnection of RF-MEMS switches. MSEM is a technique that ejects solder droplets of various diameters, and provides accuracy and a wide range of packaging applications, such as sealing rings for vacuum packaging, and fine pitch micro-solder-bump formation for the vertical interconnect and filling of via-holes to form TSV [9,10]. We have demonstrated that TSV by MSEM is applicable to wafer-level hermetic packaging for MEMS devices [10,11] and has also been applied to an RF-MEMS switch for high power handling, of which the results were partially reported [12]. In this study, we report on the detailed design, fabrication, and high frequency properties of TSV applied to RF-MEMS switches.

2. Design and fabrication of TSV by MSEM

The structure of TSV was investigated for RF-MEMS switches. The shift between signal and ground via is introduced to reduce transmission loss. The shift structures mitigate the rapid impedance mismatching caused by TSV [11]. This concept of the shift-aligned structure is applicable for any filling materials in TSV and the structure of the coplanar waveguide (CPW). Fig. 1(a) shows a calculated model of a CPW with the TSV structure. High frequency

* Corresponding author. Tel.: +81 6 6497 7533.
E-mail address: Ogawa.Shimpei@eb.MitsubishiElectric.co.jp (S. Ogawa).
[1] Present address: Department of Electrical and Electronic Engineering, Faculty of Engineering, Tottori University, 4-101 Koyama-Minami, Tottori, Tottori 680-8552, Japan.

0924-4247/$ – see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.sna.2012.04.023

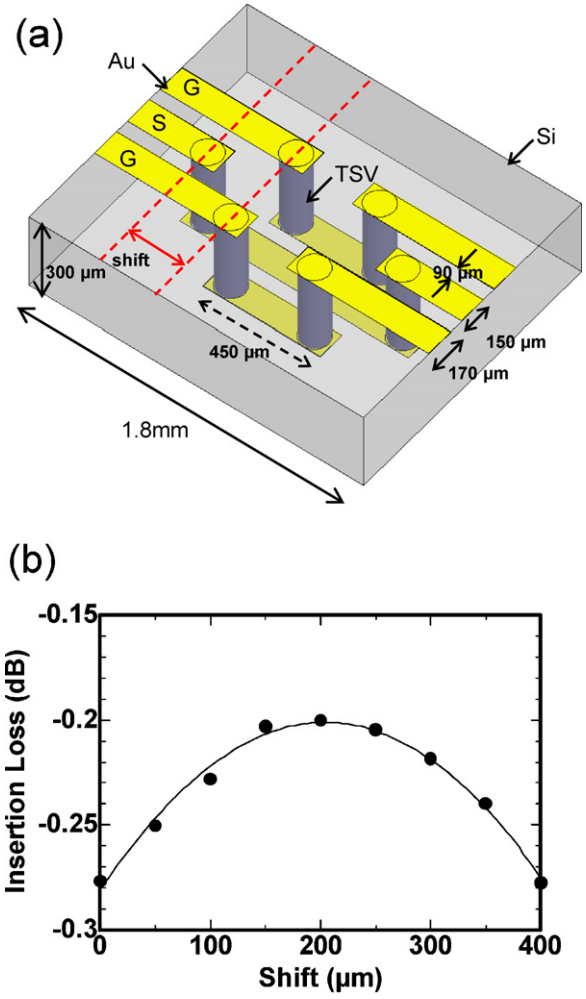

Fig. 1. (a) Schematic diagram of the shift-aligned TSV. (b) Results calculated for the insertion loss of TSV with the shift-aligned structure plotted as a function of the amount of shift.

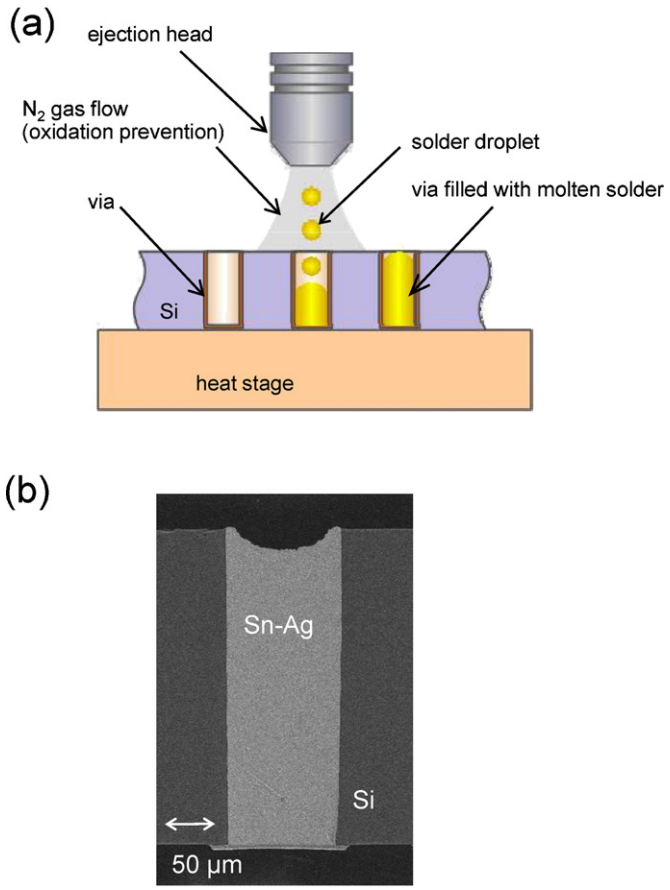

Fig. 2. (a) Schematic diagram of the MSEM and (b) cross-sectional SEM image of TSV fabricated using the MSEM.

simulations were performed using the High Frequency Structure Simulator (HFSS) from ANSYS. The diameter of the via-holes was 150 μm. The width and the distance of the CPW were designed to be 170 and 90 μm, respectively, which provides a characteristic impedance of 50 Ω. The thickness and resistivity of the Si wafer were 300 μm and 20 kΩ cm, respectively. Fig. 1(b) shows the results calculated for the insertion loss at 15 GHz as a function of the shift; a shift of 200 μm resulted in the minimum insertion loss.

Fig. 2(a) illustrates the procedure used to fabricate TSV by MSEM. The via-holes in the Si wafer are etched by deep reactive ion etching (DRIE). Ni/Au layers are sputtered on the walls of the via-holes to improve the solder wetting properties. The wafer is located on a heat stage and the solder droplets (Sn–Ag) are shot into the via-holes under a N_2 atmosphere to prevent oxidation. During solder filling, the Ni/Au and solder form intermetallic compounds [13,14]. However, the effect of the interfacial intermetallic compounds is negligible and the electrical properties of the solder are dominant, because the high frequency properties agree well with simulations [11] where only the solder is considered as the filling material and without the presence of interfacial intermetallic compounds. The diameter of solder droplets can be controlled using MSEM according to the diameter of the via-holes [9]. The MSEM is a maskless, fully dry and eco-friendly process that uses lead-free solder without a soldering flux, which is applicable for wafer-level packaging. Fig. 2(b) shows a typical cross-sectional scanning electron microscopy (SEM) image of the developed TSV fabricated using the MSEM. The solder is completely filled inside the TSV and no voids are evident in the filled solder, by which sufficient hermeticity is realized [10].

3. Fabrication of RF-MEMS switch with TSV

The fabrication procedure was developed by integrating surface micromachining and the MSEM, which required a both-sides (top and bottom side surfaces of the wafer) process. Fig. 3 shows the procedure for fabrication of the RF-MEMS switch. (i) A 20 kΩ cm and 300 μm thick Si wafer with a 1 μm thick thermal oxide layer (SiO_2) is prepared. (ii) The surface SiO_2 is etched by RIE to produce via-holes. (iii) Cr/Ni/AlSi layers (0.05/0.5/0.5 μm thick) are sputtered and patterned by ion beam etching (IBE) to form the capping layer of the via-holes. (iv) Cr/Au layers (0.02/0.2 μm thick) are sputtered and patterned by IBE to form the lower electrode and under layer of the CPW on the top side. (v) A 1.5 μm thick Ni layer is sputtered and patterned by IBE to form a sacrificial layer. In this step, the sacrificial layer remains only on the RF-MEMS switch to form the cantilever of the RF-MEMS switch. (vi) A 0.2 μm thick Au seed layer is sputtered. (vii) Thick metallization by Au electroplating with a photoresist is performed to reduce the conduction loss. Au layers (7 μm thick) are obtained to form the cantilever of the RF-MEMS switch and the CPW on the top side. (viii) The photoresist is removed. (ix) The via-holes are formed from the bottom side of the wafer by DRIE. (x) Ni/Au layers (2.0/0.5 μm thick) are sputtered to metalize the inner walls of the via-holes. The metal layers on the surface are then peeled off. Molten solder (Sn–Ag) droplets are shot into the via-holes by MSEM to obtain filled via-holes, as