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Contribution of fixed oxide traps to sensitivity of pMOS dosimeters during gamma ray irradiation and annealing at room and elevated temperature

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ABSTRACT

Gamma-ray irradiation and post-irradiation response at room and elevated temperature of radiation sensitive p-channel MOS transistors have been studied. The response was observed on the basis of threshold voltage shift determined from transistors transfer characteristics. These characteristics together with charge-pumping characteristics proved to be useful in providing a detailed insight into the processes that occur during gamma-ray irradiation and subsequent annealing at room temperature and later at elevated temperature. In particular, the influence of fixed oxide traps, switching oxide traps (known as slow switching traps) and switching traps at Si/SiO_2 interface (known as fast switching traps) on threshold voltage shift has been analyzed.

1. Introduction

Radiation sensitive p-channel MOS transistors (also known as RADFETs or pMOS dosimeter) have been developed for applications such as space, nuclear industry and radiotherapy [1–4]. The concept of pMOS dosimeter is based on the threshold voltage shift (ΔV_T) measurements and its conversion into absorbed dose rate. The increase of radiation sensitivity is one of the main goals in the design of pMOS dosimeters. This can be achieved by increasing the oxide thickness [5–9] including "sandwich" structure consisting of a layer of thermal and layer of CVD oxide [5,8,10], stacking more transistors [11,12] or applying the positive bias to the gate [8,13,14]. Besides the significant change of threshold voltage during irradiation the pMOS dosimeter must have insignificant recovery after radiation (long-term stability at room temperature) i.e. the information about absorbed radiation dose must be saved.

The pMOS dosimeter advantage over other dosimetric systems [15], include immediate non-destructive readout of dosimetric information, small size of the sensor element, the ability to permanently store the information on the absorbed dose, wide dose range, low power consumption and compatibility with microprocessor, what makes them suitable for personal dosimetry. The disadvantages are a need for calibration in different radiation fields ("energy response"), relatively low resolution (starting from about 10^{-2} Gy) and non-reusability.

In this paper we present a study of pMOS dosimeter sensitivity with thick gate oxide during gamma-ray irradiation for different gate biases, in order to inspect the experimental samples sensitivity for different operating conditions. The annealing of these dosimeters at room and further at elevated temperature of 120 °C with no gate bias has also been investigated in order to evaluate the dosimetric information for a long time period. The influence of induced charge trapping in the gate oxide and at the Si/SiO_2 interface to threshold voltage shift ΔV_T is also analyzed.

2. Experimental details

The experimental samples were radiation sensitive Al-gate p-channel MOS transistors, manufactured by Tyndall National Institute, Cork, Ireland. The transistors have 400 nm thick oxides, grown at 1000 °C in dry oxygen, and annealed for 15 min at 1000 °C in nitrogen. The post-metallization annealing was performed at 440 °C in forming gas for 60 min (see Ref. [16] for more details).

The irradiation was performed in the Metrology Laboratory of the Institute of Nuclear Science "Vinca", Vinca-Belgrade, Serbia. The samples were irradiated at room temperature using $^{60}_{27}Co$ source up to the absorbed dose of $D = 35$ Gy(Si) at the absorbed dose rate $\dot{D} = 0.02$ Gy(Si) s^{-1}. The gate bias during irradiation, V_{irr} was 0, +2.5 or +5 V. After irradiation, the samples were annealed at room temperature for 5232 h without the polarization on the gate (all pins were grounded). After that, the annealing process was continued at the temperature of 120 °C also without polarization on the gate for 423 h.

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In order to analyze the behavior of the basic mechanisms underlying radiation and post-irradiation and their influence on threshold voltage shift ΔV_T we have measured *I–V* and charge-pumping characteristics. Transfer characteristics were measured with the drain voltage −10 V, while the gate voltage step was −0.05 V. All of the characteristics were measured up to the drain current of 1 mA.

In the case of charge pumping characteristics, the triangle pulses are applied on the gate, and the average substrate (charge pumping) current I_{CP} is measured. The frequency of gate pulses was 1 MHz, the amplitude was 3 V and the signal offset varied from −6 V to 3 V. The measurements were carried out using the Keithley model 4200 SCS (Semiconductor Characterization System). System is equipped with three mediup power source measuring units (4200 SMU) used for components IV characterization. Souce measuring units have four operation voltage ranges: 200 mV, 2 V, 20 V and 200 V, while the current ranges are 100 nA, 1 μA, 10 μA, 100 μA, 1 mA, 10 mA and 100 mA. One of source measuring units is equipped with pre amplifier which provides the measurement of extrimelly low currents (order of pA). In order to perfrom charge pumping measurements, Keithley model 4200 SCS is equipped with integrated dual/channel puls generator (4205/PG2). It supports voltage pulses as short as 10 ns or up to ±20 V (into 50 Ω). Pulse amplitude can range from 100 mV up to 20 V into 50 Ω or from 100 mV up to 40 V into 1 MΩ. The programable parameters are pulse width, duty cycle, rise time, fall time, amplitude, offset. For more details see instruments datasheet.

The transistor threshold voltage before irradiation V_{T0}, as well as during irradiation and annealing, V_T ($\Delta V_T = V_{T0} - V_T$), was determined by the transfer characteristics in saturation, i.e. as the intersection between the V_G axis and the extrapolated linear region of the $(I_D)^{1/2} - V_G$ characteristics [17,18]. The densities of radiation-induced fixed traps, ΔN_{ft}, and switching traps, ΔN_{st}, were determined from the sub-threshold *I–V* curves using midgap technique (MGT) [19]. The fixed traps (FT) represent the traps created in the gate oxide that do not capture the carriers from the channel of pMOS dosimeters. Switching traps (ST) represent the traps created near and at the Si/SiO_2 interface and they do capture (communicate with) the carriers from the channel within the time frames of electrical MGT measurements [19]. The ST created in the oxide near the Si/SiO_2 interface are called slow switching traps (SST), but the ST created at the interface are called fast switching traps (FST). The charge-pumping technique (CPT) [20,21] for the determination of FST density was also used. It is known that FT cause a parallel shift of the sub-threshold transfer characteristics (MGT) or Elliot type CP curves [20] (CPT). ST result in the change of sub-threshold slope (MGT) or current (CPT).

The density of switching traps ΔN_{st}(CPT) determined by the CPT is, in fact, the density of FST (true interface traps), i.e. $\Delta N_{st}(CPT) \approx \Delta N_{fst}$. Namely, as a much faster technique, the CPT can sense only the FST and eventually just fastest among SST. The simultaneous use of both MGT and CPT is a great advantage. For instance, if ΔN_{st}(MGT) has been changed, but ΔN_{st}(CPT) has not, it means that ΔN_{sst}, i.e. the density of SST, has been changed, since $\Delta N_{st}(MGT) = \Delta N_{sst} + \Delta N_{fst}$ and $\Delta N_{st}(CPT) = \Delta N_{fst}$ [18,22].

3. Results and discussion

3.1. Irradiation

Fig. 1a gives the $\Delta V_T = f(D)$ dependence for V_{irr} values of 0, 2.5 and 5 V. The symbols in the figures represent $\Delta V_T = V_T - V_{T0}$ values obtained by extrapolation of the linear region of transfer characteristics. It can be seen that the ΔV_T values during irradiation depend on the V_{irr} values. For example, for the dose of 35 Gy the ratio of ΔV_T for $V_{irr} = 2.5$ V and $V_{irr} = 0$ V is about 2.7, while for $V_{irr} = 5$ V and $V_{irr} = 0$ V the ratio is about 4.2. It can be concluded that the polarization on the gate can cause significant influence on the range of measured gamma-ray doses. Namely, with the increase of gate bias the threshold voltage shift is higher for the same irradiation dose, what can drive the transistor away from the area of approximately linear dependence between threshold voltage shift and irradiation dose or, possibly, the transistor is much more likely to fail. Doses used in our experiments are relatively small and they do not lead to significant degradation of transistors, i.e. there is approximately linear dependence between ΔV_T and *D*.

As it was mentioned before, the application of pMOS dosimeter is based on converting the threshold voltage shift, ΔV_T, induced by radiation, into radiation dose *D*. The dependence can be expressed as [7]:

$$\Delta V_T = A \cdot D^n, \tag{1}$$

where *A* is the constant and *n* is the degree of linearity dependent on electric field, oxide thickness and absorbed radiation dose. Ideally, the dependence should be linear, i.e. $n = 1$, and in that case *A* represents the sensitivity *S*, of pMOS dosimeter:

$$S = \frac{\Delta V}{D}. \tag{2}$$

The fitting of experimental data (Fig. 1a) with the expression (1) for $n = 1$ gives the correlation factor values of 0.988, 0.996 and 0.998 for V_{irr} of 0, 2.5 and 5 V, respectively. It can be concluded that sensitivity approximation (expression (2)) is better for higher voltages applied on the gate during irradiation.

The change in areal density of FT, ΔN_{ft}, during gamma-ray irradiation for V_{irr} of 0, 2.5 and 5 V are presented in Fig. 2a. As expected the increase of absorbed radiation dose, *D*, leads to the increase of ΔN_{ft}. It can be seen that these values are bigger for the bigger values of V_{irr}.

The change in areal density of ST, ΔN_{st}(MGT), determined by MGT during gamma-ray irradiation for V_{irr} of 0, 2.5 and 5 V are presented in Fig. 3a, while the areal density of FST, ΔN_{st}(CPT), determined by CPT are presented in Fig. 4a. The data obtained by MGT and CPT are in a qualitative agreement, but ΔN_{st}(CPT) is lower than ΔN_{st}(MGT) in all cases. The difference is due to several reasons. First, two techniques have different effective frequencies: a few hertz for MGT versus 1 MHz for CPT. Both the MGT and CPT are capable of sensing the interface traps, which are very fast, but contributions for ST to MG and CP signals are not the same. While MGT sense SST and FST, the CP signals exclude SST and consequently ΔN_{st}(CPT) are expected to be lower. Second, the two techniques scan the different portions of the Si band-gap: lower half (MGT) versus central portion (CPT). As interface traps have a U-shaped distribution toward the edge of the band-gap [23,24] therefore that portion cannot be reached by CPT. This is an additional reason for lower ΔN_{st}(CPT).

The contribution of FT (ΔV_{ft}) and ST (ΔV_{st}) to the total ΔV_T is:

$$\Delta V_T = \Delta V_{ft} + \Delta V_{st}. \tag{3}$$

The FT and ST increase the ΔV_T in pMOS transistors. On the other hand ΔN_{ft} and ΔN_{st} after irradiation (or annealing) using MGT can be determined as [19]:

$$\Delta N_{ft} = \frac{C_{0x}}{q}\,\Delta V_{ft}, \quad \Delta N_{st} = \frac{C_{0x}}{q}\,\Delta V_{st}, \quad \Delta N_{ft} = \frac{C_{0x}}{q}\,\Delta V_{ft} = \frac{C_{0x}}{q}(V_{MG0} - V_{MG}); \quad \Delta N_{st} = \frac{C_{0x}}{q}\,\Delta V_{st} = \frac{C_{0x}}{q}(V_{S0} - V_{S0}(0)), \tag{4}$$

where C_{0x} is the capacitance per unit area and *q* is the absolute value of electron charge, V_{MG0} is the midgap voltage before irradiation, V_{MG} is the midgap voltage after irradiation or annealing, $V_{S0}(0)$ is the value of stretch-out voltage before irradiation and V_{S0} is the value of stretch-out voltage after irradiation or annealing.