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Sharp silicon/lead zirconate titanate interfaces by electrophoretic deposition on bare silicon wafers and post-deposition sintering

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ABSTRACT

Thick films of Nb-doped lead zirconate titanate (PZT) on bare silicon (Si) wafers were prepared by electrophoretic deposition (EPD) in ethanol-based suspensions. Alloyed Al/Si ohmic contacts were used for electrical connections. EPD on bare Si wafers was obtained with similar results to metallic substrates, at nominal electric fields between 4350 and 10900 V m^{-1}. Well-adhered and crack-free green films were obtained after solvent evaporation. Sintering of green PZT films was performed at either 850 °C or 950 °C for 1 h. Sintered PZT films on Si featured sharp Si/PZT interfaces and a good degree of crystallinity. Possible applications of sintered PZT/Si structures as on-chip sensors are discussed, taking into account relevant literature results.

1. Introduction

The integration of piezoelectric lead zirconate titanate (PZT) films on Si wafer has been actively pursued over the past decade. Integration of PZT on silicon wafer is sought after for many reasons. Single-crystal Si wafers are used in the electronic industry to produce a broad array of low-cost on-chip devices, whereby electric signal generation and processing can be obtained. PZT piezoelectric ceramics – both in bulk and film form – are ideal materials for sensors and actuators due to their large piezoelectric constants. Piezoelectric sensors provide a voltage signal that is proportional to the applied stress, which can be fed as input to external circuitry for analogue or digital processing purposes (amplification, signal re-shaping, A/D conversion, etc.). Direct integration of the piezoelectric material on Si wafer is obviously attractive, in that it allows, at least in principle, the fabrication of compact structures on silicon chips providing both the sensing functions and the analogue processing of the sensor's raw signal. Conversely, by coupling VLSI/ULSI electronic circuitry to active piezoelectric ceramic films on the same silicon chip, microactuators may be produced whose driving analogue voltage signal would be generated on the same chip.

Piezoelectric ceramics can be deposited on a solid substrate by means of a number of techniques. Amongst these, screen-printing appears to be favoured. Screen printing is carried out by smearing a ceramic powder paste on the substrate through a screen of woven mesh. The shape of the patch of paste being transferred onto the substrate is controlled by masking the screen, whilst the thickness of the deposit can be controlled by depositing as many layers as needed. Screen printing is a rheology-controlled process, since the way the paste is transferred onto the substrate through the screen depends on its rheological parameters, such as viscosity and thixotropy.

In the last years, electrophoretic deposition (EPD) has been increasingly used for the formation of thick and thin ceramic films [1], due to good properties of the deposits and easy control of their thickness and texture. EPD of ceramic materials is performed by polarizing conductive electrodes in stable colloidal suspensions of ceramic powders. Since colloidal particles are electrically charged, establishing an electric field between two conductive electrodes causes them to move towards one of the electrodes, on which they deposit. Both DC and AC [2] polarization have been employed for EPD purposes. The thickness and texture of such deposits can be controlled by varying the deposition conditions and the physical state of the colloidal suspension, in particular the voltage applied to the deposition cell, the deposition time and the zeta potential of the particles. EPD has been applied to the deposition of PZT ferroelectric ceramics, both from colloidal suspensions of pre-sintered PZT powders [3–6] and colloidal suspensions of oxide mixtures (PbO, ZrO_2 and TiO_2) [7].

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Whilst the fabrication of extremely complex electronic circuitry on silicon wafer by VLSI and ULSI is a well-established industrial process, the integration of piezoelectric material on silicon wafer may pose problems. To obtain a sturdy and fully functional sensor/actuator structure on silicon wafer, able to withstand for a reasonably long time the cyclic mechanical loading and the detrimental effects of fatigue typical of sensor/actuators applications, the mechanical stability of the Si/PZT interface must be very high. First and foremost, a very good adhesion between the piezoelectric film and the silicon substrate is required. Moreover, two conductive electrodes are needed to either sense the voltage that develops across a piezoelectric element when it is mechanically loaded (sensor mode) or to apply the required driving voltage to the same (actuator mode). One of the two electrodes (bottom electrode) is usually placed between the silicon substrate and the piezoelectric, thus making the Si/metal/piezoelectric stack the standard configuration for on-chip piezoelectric devices. Whilst needed, the bottom electrode is obviously a weak link of the structure as to mechanical stability, since stress-induced delamination is likely to occur at the Si/metal interface and/or the metal/PZT interface. To improve the adhesive and mechanical performance of the stack, many strategies have been used. Ti/Pt metallic bilayers, with Ti acting as the adhesion layer (usually about 10–20 nm thick) are known to strongly pin to Si/SiO_2 surfaces, and have been used in the fabrication of electrical devices based on ferroelectric/silicon architectures [8]. Other materials may be present in the structure, amongst which Si_3N_4 [9]. However, high-temperature (HT) processing of such structures often leads to the delamination at the silicon/ferroelectric interface, thus destroying the structure [10]. Two post-deposition HT steps are required to bring a piezoelectric film to its full functionality, namely sintering and poling.

On both bulk and thick film piezoelectrics, sintering (also referred to as densification) is required to achieve a good degree of crystallinity of the material. On bulk piezoelectric specimens obtained by powder pressing, sintering can be conducted at temperatures as high as 1200 °C, but when thick and thin piezoelectric films on a substrate come into play it is usually performed at a somewhat lower temperature.

As a rule of thumb, the higher the sintering temperature the better is the degree of crystallinity and, in turn, the piezo performance of the sintered material. In the case of piezoelectric films, however, trade-off considerations must be made, since HT sintering of Si/Metal/PZT stacks can heavily damage the structure. Therefore, a range of sintering aids are mixed to the piezoelectric material to help densification at lower temperatures. Firing temperatures as low as 700 °C are occasionally reported in the literature for PZT when a sintering aid is used [11].

Since Pb is a volatile element, PZT sintering must take place in a lead-saturated environment, because loss of Pb by evaporation at high temperature (HT) leads to a worsening of its piezoelectric performance. PZT has been shown to react at high temperature with Si/SiO_2 substrates leading to the formation of surface microstructures [10] that are not compatible with proper working of the device. It has been found that lead diffusion in the Si wafer cannot easily be stopped by using barrier layers, and that delamination and buckling of the bottom electrode often occurs [10]. On the other hand, the strong concentration gradients that are typical of stacked structures bring about a complex interdiffusion pattern as soon the temperature is brought to a high enough value to cause the mobilization of the diffusing species. This too may lead to a degradation of the piezoelectric performance, due to poisoning of the piezoelectric layer. The problem is aggravated if a high number of layers are present in the stack, for adhesion, electrical conductivity or diffusion barrier purposes.

Poling is performed by applying a strong electric field across the material whilst the latter is kept above its Curie temperature. Poling is needed to achieve proper orientation of the piezoelectric domains in the material. A top metallic electrode must be deposited on the material both for poling and to tap the piezoelectric signal during device operation. Once the orientation of the piezoelectric domains has been achieved, the material is cooled down to room temperature (RT) whilst keeping the field on, thus freezing the oriented configuration. The poling step brings the material to its full piezoelectric performance, and is performed at temperatures about 150 °C. Due to the lower temperature, the poling step is less damaging to the stacked structure than the sintering step.

Besides being a critical part of the stack, the fabrication of a complex-structured bottom electrode – including adhesion and barrier layers – is a costly process, due to the widespread use of noble metals (Au, Pt) and to their deposition on the wafer by time- and labour-intensive techniques such as high-vacuum (HV) evaporation and sputtering. Based on the above observations, the bottom electrode is easily singled out as the most taxing component of the stack. Any novel procedure to fabricate working PZT/Si on-chip devices without a metallic bottom electrode would be a major improvement in the field, both from a processing point of view and the improvement of the mechanical coupling between the PZT layer and the Si substrate. Experiments performed in this Laboratory made it clear that it is possible to produce EPD films – having thickness in the range of a few tens of μm – by electrophoretic deposition of PZT directly on bare Si wafer. Appropriate post-deposition thermal treatment of such films can produce neat Si/PZTN interfaces that appear to be strongly adhered to the silicon substrate. A description of the procedures used to obtain sintered EPD-PZT films on bare silicon wafer is presented in this paper. SEM/EDX and XRD observations of the sintered Si/PZT interface are reported. Finally, the possibility of using such EPD-PZT/Si structures as sensors is discussed.

2. Experimental

1530-μm-thick Si wafer (dopant unknown) was used as the substrate for the EPD of Nb-doped lead zirconate titanate (PZTN). Rectangular wafer cuttings (0.6 cm × 4 cm approx.) were produced using a Berney T34 precision saw. Due to the thickness of the wafer, cleaving proved to be unpractical. No metallization was deposited on the Si substrates.

Ohmic contacts to Si were prepared by HT Al/Si direct reaction alloying [12]. The silicon wafer was firstly chemically cleaned by boiling in concentrated (65%) nitric acid for 30 min [13]. The contacts were obtained by introducing each Si substrate loaded with two Al pellets in a furnace, and then bringing the temperature to 700 °C at 100 °C/h. A 1-h stay at 700 °C was subsequently allowed, followed by natural cooling. The 1-h temperature plateau in the thermal cycle was chosen at a somewhat higher temperature than ~580 °C (prescribed by Ref. [12]) due to better results as to linearity and low electrical resistance of the so obtained ohmic contacts. To enable testing of the ohmic contacts, two such contacts were fabricated on each slab, and a linear voltage sweep was applied across them using an Eco Chemie μAutolab Type III/FRA2 electrochemical workstation. The potential was swept from the negative to the positive region to rule out Schotty barrier (i.e. diode-like rectifying) behaviour of either Al/Si contact on the slabs. *I–V* curves were recorded to check for linearity (purely resistive behaviour), and to estimate the bulk Si resistance. Since the whole thermal cycle was performed in air, SiO_2 growth occurred on the surface of the slabs. Due to SiO_2 being a very effective electrical insulator, a subsequent oxide removal step by alkaline etching was performed to allow free electrical charge transfer during EPD.

Alkaline etching of thermally grown SiO_2 was performed by dipping the Si substrates in 2 M aqueous KOH at 55–60 °C for 1800 s.