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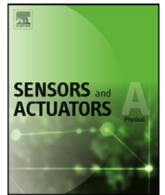

CMOS compatible polycrystalline silicon–germanium based pressure sensors

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ABSTRACT

This work demonstrates, for the first time, the use of poly-SiGe for the fabrication of both piezoresistive and capacitive pressure sensors at CMOS-compatible temperatures. Despite the low processing temperature (455 °C), a sensitivity of 4.6 mV/V/bar for a membrane of $200 \times 200\ \mu m^2$ is reached by piezoresistor design optimization. The possibility of further enhancing the sensor sensitivity by tuning the piezoresistor's annealing time is investigated, leading to a 30% improvement. Single capacitive pressure sensors with sensitivities up to 73 fF/bar have been successfully fabricated. Annealing tests, performed at a fixed temperature of 455 °C with different annealing times, prove that the presented pressure sensor process flows are compatible with post-processing above 0.13 μm Cu-backend CMOS devices. The increase in metal-to-metal contacts (more than 8% after 6 h annealing), rather than transistor performance or degradation of the metal interconnects, is what limits the post-processing thermal budget.

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1. Introduction

The monolithic integration of the micro-electromechanical systems (MEMS) with the driving, controlling and signal processing electronics on the same Complementary Metal Oxide Semiconductor (CMOS) substrate can improve performance as well as reduce assembly and packaging cost [1]. The post-processing route (fabricating MEMS directly on top of CMOS) is the most promising approach for CMOS–MEMS monolithic integration as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes. However, for above-CMOS integration, the MEMS fabrication thermal process budget must be carefully designed in order to avoid introducing any damage or degradation in the performance of the existing electronics or interconnects [2,3]. For this reason, high quality polycrystalline Si (poly-Si), the most commonly used material for surface micromachined MEMS pressure sensors, is not a suitable candidate for above-CMOS integration since it requires high temperature annealing for stress reduction and dopant activation. Polycrystalline silicon–germanium (poly-SiGe) has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing post-processing on top of CMOS.

Recently, an alternative technology to fabricate MEMS devices on top of CMOS has been reported. It is based on the use of the top CMOS metal interconnect layers to fabricate the MEMS device [4,5]. This technique, although cost efficient, does not offer flexibility in the design. The thickness of the metal layers, used as MEMS structural layers, will be fixed by the CMOS foundry. Moreover, the use of metals as structural layers might not be ideal for certain applications, like pressure sensors, as metals often suffer from creep. This technique is also not suitable for piezoresistive pressure sensors.

Poly-SiGe, on the other hand, offers a generic and flexible technology for above CMOS integration. Since the MEMS fabrication can be completely decoupled from the CMOS fabrication, the designer is no longer limited by the CMOS foundry, and the MEMS dimensions can be optimized based on the application requirements. With poly-SiGe it is also possible to monolithically integrate multiple sensors with the electronics, enabling sensors measuring motion along different axes to be precisely aligned, to have greater accuracy and to be less susceptible to external disturbance. Several poly-SiGe MEMS devices, including micromirrors and resonators, have already been presented [6,7]. Recently, thin film packaging has been added into IMEC's poly-SiGe MEMS-last technology [8,9]. Moreover, recent experiments demonstrated the piezoresistive properties of poly-SiGe [10], broadening the possible applications of this material to the MEMS piezoresistive sensor market.

In this work, for the first time, both capacitive and piezoresistive poly-SiGe-based pressure sensors are fabricated and tested. The maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460 °C to

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enable above-CMOS integration. The effect of annealing time on the piezoresistive pressure sensor performance was also studied. Finally, in order to evaluate the compatibility of the proposed process flow with above-CMOS post-processing, annealing tests are performed on CMOS wafers fabricated using 0.13 μm technology with copper (Cu) backend. This represents the first experimental evaluation of the degradation introduced by the MEMS thermal budget in the performance of CMOS wafers with copper interconnects.

2. Poly-SiGe piezoresistive pressure sensors

2.1. Design

Piezoresistive pressure sensors with four different designs of piezoresistors were implemented (Fig. 1). A constant membrane area ($200 \times 200\,\mu m^2$) is used for all the designs. The first two designs present simple "single-line" longitudinal resistors while the last two designs have "n-shape" longitudinal resistors. Also, in two of the designs the transverse piezoresistors are placed in the center of the membrane instead of at the edge, as usual. This is expected to improve the sensitivity by a factor of around 2 [10]. To better understand this, finite element simulations of the stress distribution on a $200 \times 200\,\mu m^2$ and 4 μm-thick poly-SiGe membrane subjected to an external pressure of 1 bar were performed (Fig. 2). From this figure we can observe that the stress is high at the center and in the areas near the middle edge of the membrane. Also, the stress is tensile (positive) at the edge of the membrane and compressive (negative) in the center.

From [10] we know that the longitudinal gauge factor of boron-implanted poly-SiGe is much larger than the transverse gauge factor, and that, for the boron concentration considered in this work, both the longitudinal and transverse gauge factors are positive. Therefore, in order to achieve better sensitivity, the piezoresistors should be arranged in such a way that they will experience maximum longitudinal stress (σ_{yy} in Fig. 2). Moreover, as the 4 piezoresistors are placed in a Wheatstone bridge configuration, the sensor output voltage is proportional to the difference between the relative resistance variation of the longitudinal (R_l) and transverse (R_t) piezoresistors ($V_{out} \propto (\Delta R/R_l - \Delta R/R_t)$); therefore a negative resistance variation for the transverse piezoresistors would result in an increased sensitivity (assuming a positive $\Delta R/R_l$). From all this we can conclude that by placing the transverse piezoresistors in the center of the membrane, where a higher and negative longitudinal stress is found, the sensitivity can be improved as compared to the more traditional piezoresistor placement (at the left and right edge, where the longitudinal stress is low and positive).

2.2. Fabrication

The general fabrication process for the piezoresistive pressure sensors is schematically illustrated in Fig. 3. A standard 8-in. diameter Si wafer with (1 0 0) orientation is used as the starting substrate. A 3-μm thick High Density Plasma (HDP) Si-oxide layer, to be used as sacrificial material, is deposited at 400 °C (required time is ~6 min). This oxide layer is patterned and plasma-etched, stopping in the underlying Si substrate to define the anchor region. Only one anchor width of 1 μm is used to ensure a planarized membrane layer after deposition. The total anchor region width surrounding the membrane is 25 μm for all designs.

The B-doped poly-SiGe structural layer was then deposited at 460 °C chuck temperature (450 °C wafer temperature) by a combination of Chemical Vapor Deposition (CVD) and Plasma Enhanced CVD (PECVD). An annealing step of 30 min at 455 °C is performed before the SiGe deposition to ensure a proper outgassing of the underlying layers, avoiding the formation of bubbles later on. The CVD and PECVD are both performed in an Applied Materials PECVD Centura CxZ chamber. The PECVD SiGe layer is deposited on top of a polycrystalline CVD SiGe seed layer (~400-nm thick) to induce crystallization in the PECVD layer [11]. The maximum thickness of PECVD SiGe that can be deposited before a chamber clean is required is ~2 μm. If a thicker layer is needed, PECVD layers can be stacked until the final thickness is reached. In this case, a 30 s CF_4 clean is performed before each extra PECVD to remove any unwanted oxide at the PECVD/PECVD interfaces [12]. The final SiGe layer used in this work is build by stacking a CVD seed layer and 2 PECVD layers, leading to a total thickness (estimated from cross-section pictures) of ~3.2 μm. The silicon gas source is pure silane, whereas 10% germane in hydrogen has been used as the germanium gas source. The total deposition time for the SiGe structural layer is ~40 min.

To define the piezoresistors, a 200-nm thick CVD poly-SiGe layer with a Ge content of 77% (determined by a Rutherford Backscattering analysis) was deposited. The deposition temperature and time for the piezoresistive layer are 450 °C (wafer temperature) and ~12 min, respectively. A thin silicon carbide (SiC) layer was used as isolation layer between the SiGe membrane and the SiGe piezoresistors (Fig. 4a). After deposition, the poly-SiGe film was doped through ion implantation of boron at 35 keV with a dosage of $2 \times 10^{14}\,cm^{-2}$ (concentration $1 \times 10^{19}\,cm^{-3}$). This boron concentration resulted in the highest gauge factor in our previous work [10] and was therefore the one selected for the piezoresistive layer in this pressure sensor. After implantation, the wafers were annealed in a conventional furnace for 2 h at 455 °C for dopant activation.

After patterning the piezoresistors, release holes of nominally $1 \times 1\,\mu m^2$ were etched in the membrane (Fig. 4b). In order to reduce the time required to etch away the sacrificial layer, and also preventing in this way attacking the anchor region, etch ports are opened in the membranes on top instead of using lateral etch paths. The size of the release holes was selected to be large enough to enable efficient sacrificial etching but, at the same time, small enough to limit both the required thickness of the sealing layer and the quantity of sealing material deposited on the interior surfaces of the cavity.

To avoid stiction during release, anhydrous vapor HF (AVHF) together with ethanol vapor [13] is used to etch the sacrificial oxide inside the cavities. The use of an alcoholic vapor, such as ethanol, as a catalyst instead of water vapor is explained as a way to minimize residue product and process-induced stiction [14]. The release process is performed in 8 steps of 8 min on a Primaxx Clean Etch Technology (CET) tool. Breaking down the release time in steps has several advantages. The most important is the reduced chance for stiction as water, which is a byproduct of the etching process, can be removed easily when the release time is broken in steps.

After release, the membranes were sealed using a ~1.2-μm thick Sub-Atmospheric CVD (SACVD) oxide layer deposited at 420 °C (Fig. 5). The total deposition time for the sealing oxide is 7.3 min. To verify the sealing process, the membrane deflection was measured on similar test devices by white light interferometry using an optical interference profilometry system (Wyko NT3300) [15,16]. The measurements were performed for two different pressures: 1 bar (atmospheric pressure) and ~0.25 bar (Fig. 6). The difference in membrane deflection under the two pressures considered indicates that the membranes are sealed.

Finally, in order to provide electrical contact to the piezoresistors, $1 \times 1\,\mu m^2$ vias were etched in the sealing oxide on top of the piezoresistors. After etch, these contacts are filled with a Ti (20 nm)/AlCu (880 nm)/TiN (60 nm) metal stack deposited at 350 °C. Fig. 7 shows a top-view of a fabricated device.

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