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Highly efficient piezoelectric micro harvester for low level of acceleration fabricated with a CMOS compatible process

M. Defosseux [a,*], M. Allain [a], E. Defay [b], S. Basrour [a]

[a] TIMA Laboratory (CNRS-Grenoble INP-UJF), 46 av. Felix Viallet, 38031 Grenoble Cedex, France
[b] CEA LETI Minatec Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

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ABSTRACT

This paper reports on the fabrication and characterization of piezoelectric micro-harvesters vibrating at 200 Hz for acceleration lower than 0.25 g (1 g = 9.81 m s^{-2}). A CMOS compatible process involving Aluminum Nitride (AlN) thin films was developed on Silicon On Insulator (SOI) substrate. A typical device exhibits a volume of 2.8 mm^3, harvests 0.62 μW at 214 Hz and 0.25 g as input acceleration. The harvested power reaches the same level under vacuum but at only 0.15 g. This result confirms that using a packaging under vacuum for piezoelectric energy harvesters is very interesting in order to improve the efficiency for a given acceleration. Finally, it turns out that our devices exhibit the highest Mitcheson figure of merit in the 0–1 kHz range, namely 12.2%.

1. Introduction

There is nowadays a huge interest in vibrating energy harvesting. By taking advantage of the decreasing power consumption of wireless sensors networks nodes, the idea is to power them with the surrounding energy, instead of using batteries. If ambient energy is used, the maintenance of batteries would be avoided. Vibration ambient energy harvesters are a promising solution for this problem [1–3]. These nodes can be spread in an environment in order to collect a high density of information [4,5]. The ultimate goal is to have a system on chip or in package for each node with sensors, energy harvesters, electronics and a transceiver. To be able to obtain such a system, the harvesters have to be micro-fabricated to achieve a low volume.

In order to power sensors network nodes with mechanical energy of vibration, it is necessary to convert this energy to electricity. Three methods are available for this conversion: electromagnetic, electrostatic and piezoelectric. Devices using the piezoelectric conversion can be miniaturized, and can exhibit high conversion efficiency and high power output [6–8]. We have therefore chosen to develop a piezoelectric vibration energy harvester.

Piezoelectric energy harvesters are usually resonant structures. They are generally constituted by a clamped free beam with a seismic mass in order to reduce the resonance frequency. A part of the beam is made of piezoelectric material to convert mechanical energy into electrical energy. Microsystem fabrication techniques are useful to perform miniaturized devices. Contrarily to their macroscopic harvesters counterparts, thick piezoelectric ceramics are not desired for microsystems [6,7]. Generally speaking, piezoelectric energy micro-harvesters exhibit a silicon-piezoelectric thin film structure, as depicted in Fig. 1.

Piezoelectric harvesters are more efficient close to their resonance frequency. Besides, most of the vibrations in the surroundings take place at low frequency, below 200 Hz [1]. Moreover, microsystems mean small devices and therefore devices in the mm^3 range are desired. Indeed, the order of magnitude of the minimum power needed to power a node is 0.5 μW [9]. As a consequence, piezoelectric harvesters should exhibit a resonance frequency below 200 Hz together with a volume in the mm^3 range. These two requirements are difficult to reach simultaneously because the downscaling of the dimensions leads naturally to an increase of the resonant frequency of the devices.

In this paper, a piezoelectric harvester with dimensions in the mm^3 range is proposed with a resonance frequency around 200 Hz, SOI substrate and CMOS compatible deposition techniques. In the first section, the design of the device is presented. Then, the fabrication process is detailed followed by the characterization results. Finally, our results are compared with the literature by using Mitcheson's figure of merit [3].

2. Design

Usually, Lead Zirconate Titanate (PZT) is used as piezoelectric material for harvesters as it exhibits piezoelectric coefficients 20

* Corresponding author. Tel.: +33 476574304; fax: +33 476574981.
E-mail address: maxime.defosseux@imag.fr (M. Defosseux).

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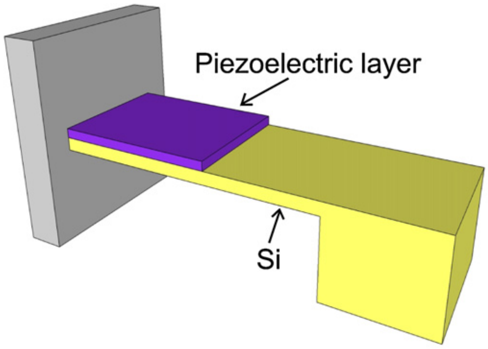

Fig. 1. Structure of a piezoelectric energy micro-harvester.

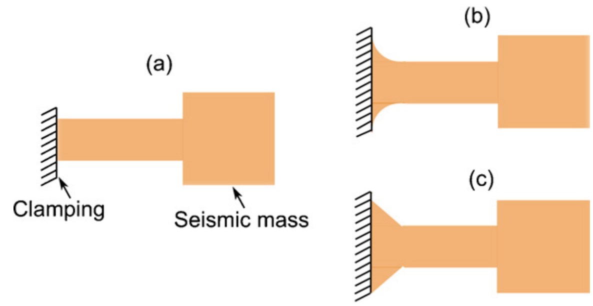

Fig. 2. Three different shapes of the clamped region for the harvester: (a) straight, (b) rounded, and (c) trapezoidal.

times higher than AlN. However, AlN has a permittivity 100 times smaller than PZT [10,11]. Therefore, by taking into account piezoelectric coefficients over permittivity ratios, AlN exhibits an output voltage ten times higher than PZT for a given mechanical stimulus. This has a huge impact on the collected energy, as voltage is the preferred mode of energy collection. Indeed, diode bridges are often utilized after the harvesting device and higher voltages are useful to neglect the usual 0.7 V built-in potential of diodes.

Priya [12] defines a figure of merit (FoM) to compare the efficiency of piezoelectric layers. This FoM reads:

$$\mathrm{FoM} = \frac{d_{31}^2}{\varepsilon_{33}\ \tan\delta} \quad (1)$$

d_{31} is the transverse piezoelectric in $\mathrm{C\,N^{-1}}$, $\tan\delta$ the dielectric losses and ε_{33} the permittivity in $\mathrm{F\,m^{-1}}$. This FoM is suitable for a transverse mode energy harvester. Usually, this transduction mode is utilized in flexural structures, as the device depicted in Fig. 1. Note that this FoM corresponds to thin films as no material stiffness is taken into account. The basic assumption is that all compared materials are films deposited on a substrate. Those films are supposed to be thin enough in order to neglect their stiffness compared to the substrate's one. The performances of thin layers of PZT and AlN published in the literature are reported in Table 1. Thanks to its low dielectric losses, AlN appears to be more interesting than PZT despite its lower piezoelectric coefficients. Note that $\tan\delta$ has to be taken into account especially in the case of the resonance, which is the case we are interested in.

Technology wise, AlN needs only 400 °C to be grown in its desired wurtzite crystalline, whereas PZT requires 650–700 °C. Moreover, AlN is lead free, which is a clear advantage for integration with CMOS process.

As already discussed, a high output voltage is desired. Therefore, increasing piezoelectric film thickness is beneficial as it decreases the capacitance of the device and consequently increases the voltage for a given mechanical stimulus [9]. 2 μm-thick AlN films are maximum we could deposit in our sputtering tool.

In order to improve the maximum strain sustainable by the harvester, different shapes were implemented. As shown in Fig. 2, three kinds of clamped-free beams were designed. All designs exhibit a cantilever attached to the holder followed by a seismic mass at the free end. The different designs are related to the cantilever clamped region that exhibits different shapes: straight (a), rounded (b) and trapezoidal (c). The goal of circularly filleted and trapezoidal beams is to spread spatially the maximum of stress at the clamping. It was shown in a previous study [13] that this approach increases the tolerance to high acceleration of the device.

Table 1
Comparison of performances of PZT and AlN piezoelectric thin layers.

Material	$\varepsilon/\varepsilon_0$	d_{31} (10^{-12} m V^{-1})	$\tan\delta$ (%)	FoM (10^{13} m^2 C^{-1})	Ref.
PZT	935	−110	3.6	4	[10]
AlN	10	−2.6	0.1	7.8	[11]

The dimensions of the structure were designed according to the desired resonance frequency. An analytical model [9] together with Finite Element Modeling (FEM) simulations was utilized. As an example, Fig. 3 shows the FEM mesh of a rounded shape harvester. The material parameters used are given in Table 2. Some dimensions were imposed by the fabrication process: 500 μm-thick seismic mass, beam thickness of 14–12 μm of silicon and 2 μm of AlN. The in-plane dimensions of the structure were chosen to obtain a device strong enough at the resonance frequency of 200 Hz to withstand an input acceleration of 0.25 g. The high efficiency of the device was obtained by defining the maximum stress level in the device close to the maximum stress that every material can withstand in the stack.

3. Fabrication

The fabrication process flow is shown in Fig. 4. It was developed partly on 200 mm wafers (stack deposition) and 100 mm wafers (pattern and release). The initial wafers were 200 μm-SOI wafers with 500 μm-thick substrate, 1 μm-thick buried SiO_2 and 10 μm thick SOI thickness (Fig. 4.1). First, 100 nm-Mo bottom electrode was sputtered followed by 2 μm-thick AlN films deposited by dc-pulsed reactive sputtering. The top electrode is made of 100 nm-thick sputtered Pt (Fig. 4.2). The rest of the technology was developed on 100 mm wafers. A laser process was performed to obtain two 100 mm-wafers out of each 200 mm wafer. Pt was etched by Ion Beam Etching (Fig. 4.3) whereas AlN was etched using H_3PO_4 at 110 °C (Fig. 4.4). Mo was etched by Reactive Ion Etching by using SF_6 (Fig. 4.5). Then, 100 nm-thick Au was deposited and patterned by lift-off (Fig. 4.6) to improve the contact quality on Mo. An aluminum hard mask for the deep etching of the seismic mass was sputtered and patterned by wet etching (Fig. 4.7–4.8). The beam was therefore patterned by etching SOI Si by Deep Reactive Ion Etching (DRIE) (Fig. 4.9). Finally the backside was patterned by a DRIE in order to define the seismic mass. This was the most critical step as 500 μm have to be etched. The last step was the release

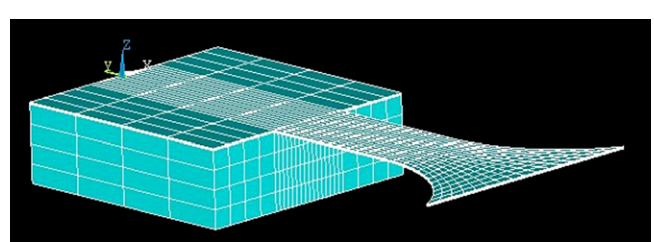

Fig. 3. Rounded harvester meshed by the FEM software.