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Characterization of intermediate In/Ag layers of low temperature fluxless solder based wafer bonding for MEMS packaging

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ABSTRACT

Low temperature fluxless solder for wafer bonding has received a lot of attention due to its great potential in hermetic MEMS packaging. Previous research activities mainly deploy solder alloy of eutectic composition to achieve low bonding temperature. We proposed new intermediate bonding layers (IBLs) of rich Ag composition in In–Ag materials systems. In this study, we investigated the intermetallic compounds (IMCs) at the bonding interface with respect to the bonding condition, post-bonding room temperature storage and post-bonding heat treatment. With this IBL, the IMCs of Ag_2In and Ag_9In_4 with high temperature resist to post-bonding process are derived under process condition of wafer bonding at 180 °C, 40 min and subsequent 120–130 °C annealing for 24 h. Low melting temperature IMC phase of $AgIn_2$ is formed in the interface after long term room temperature storage or 70 °C aging treatment. This low melting temperature IMC phase can be completely converted into high melting temperature IMCs of Ag_2In and Ag_9In_4 after 120 °C additional annealing. Based on our results, we can design the packaging process flow so as to get reliable hermetic packaged MEMS devices by using low temperature fluxless In–Ag wafer bonding.

1. Introduction

Transducer mechanisms, structures, materials and fabrication technologies for microelectromechanical system (MEMS) devices change depending upon their applications. The MEMS packaging technologies remain as application-specific solutions [1,2]. Thus the packaging of MEMS devices is considered as the most challenge tasks of MEMS commercialization. The MEMS packaging technology typically is categorized as two groups in terms of wafer scale and chip scale. The main consideration is that the free-standing and fragile MEMS structures either have to be protected properly before the chip singulation step, e.g. saw dicing, or must be strong enough for withstanding saw dicing step. General speaking, suitable technologies for MEMS packages typically need to provide sealing or encapsulation of MEMS structures, electrical feedthroughs and pathways of that MEMS devices can interact with ambient so as to either sense the change or introduce a change. Wafer scale packaging is considered as the lower cost approach than chip scale solution typically because it may offer sealing and electrical feedthroughs via wafer bonding step. Thus various wafer bonding technologies have been investigated for MEMS packaging applications. These wafer bonding technologies are categorized as two approaches, i.e., direct bonding and in-direct bonding, i.e., the intermediate layer bonding. The direct bonding approach include technologies such as, silicon fusion bonding at about 1000 °C [3], Si/glass anodic bonding at about 450 °C [4], plasma surface activated bonding at 450 °C in vacuum [5] and even at room temperature in vacuum [6] and in ultrahigh vacuum [7]. On the other hand, the choice of the intermediate bonding layer (IBL) will be made according to the type of substrates to be bonded and whether there is a requirement of hermetic sealing or not. The well-known intermediate layer bonding are polymer based bonding at temperature ranging from 100 °C to 150 °C [8,9], Au/Sn solder based eutectic bonding at 280 °C [10,11], Au/Si eutectic bonding at 365 °C [12], and glass frit bonding at 400 °C [13,14]. In view of most of applications that need to have the hermetical sealed packages, polymer based intermediate layer bonding has gas permeable interface and does not meet the hermetic sealing requirement. Therefore, Au/Sn solder bonding

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and glass frit bonding are the main stream approaches in MEMS industry nowadays.

Besides a lot of MEMS devices contain different materials or need to bond substrates containing the electronic part of the devices (e.g. CMOS wafers). Thus the difference in thermal expansion coefficients of the dissimilar materials results in a mechanical stress in proportion to process temperature. It points out that low temperature wafer bonding technology is a key for avoiding such residual mechanical stress due to aforementioned reasons.

To fulfill the hermetic sealing and low process temperature, Indium and indium-based alloy solders have been reported to be very attractive intermediate layer materials. Since the In–Sn material system has eutectic point at 118 °C and pure indium is melted at 156.6 °C. Several literatures have reported the chip-to-chip low temperature bonding by using In–Sn, In–Ag, In–Cu and In–Au [15–20], while the wafer level packaging using In–Sn eutectic solder bonding [21] and In compression bonding [22–24] have been reported. Moreover, industry also requires that the formed solder-bonded interfaces can be survived at temperature at least as high as 285 °C which is the peak temperature in the surface mounting technology (SMT) manufacturing line. It means that the resulted intermetallic compounds (IMCs) of the solder-bonded interfaces in any post-bonding steps need to have melting temperature, i.e., defined as re-melting temperature, higher than the post-bonding process temperature. In this paper, we are working on In–Ag low temperature solder based wafer bonding with aim of materials evolution of the resulted IMCs at the bonded interfaces with respect to various post-bonding heat treatment process condition.

2. Intermediate bonding layer design and experimental condition

As we described in introduction, it is very intriguing to develop reliable metallurgy using In–Ag materials system for wafer level MEMS packaging. In the In–Ag phase diagram (Fig. 1) [25], the eutectic temperature is observed as 144 °C at 96.5 wt.% In, while the melting temperature of indium and silver is referred to 156.7 °C and 961.9 °C, respectively. Chuang and Lee have reported that In–Ag chip-to-chip is successfully bonded at temperature slightly above 200 °C and with additional 150 °C annealing in hydrogen environment [17]. The derived bonding interface shows high re-melting

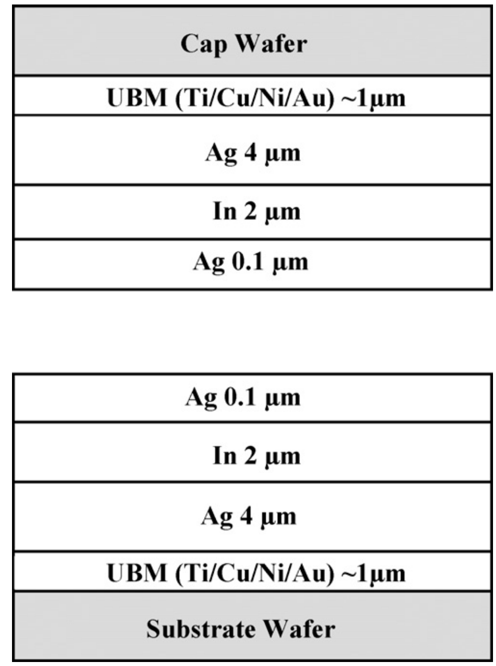

Fig. 2. The intermediate bonding layers on both sides of bonding pair wafers, where the schematic drawing showing thin silver coated surface of both sides are face to face arranged.

temperature. It points out that the resulted bonding interface was produced by consumption of all the indium in the bonded couple to form Ag_2In IMC phase.

More clearly speaking, reliable bonding can be realized by a fluxless soldering approach that comprises IBL combinations including a low melting point (LMP) component, e.g. In or Sn, and a high melting point (HMP) component, e.g. Au, Ag, or Cu. Without using the eutectic composition, e.g. 96.5 wt.% In of In–Ag system, the HMP/LMP ratio of overall IBL is selected to be higher enough. Therefore the LMP component is essentially depleted into HMP layer and reacted into an IMC that has a higher melting temperature, i.e., the re-melting temperature, than the original melting temperature of LMP component. Thus, as shown in Fig. 2, we propose an IBL com-

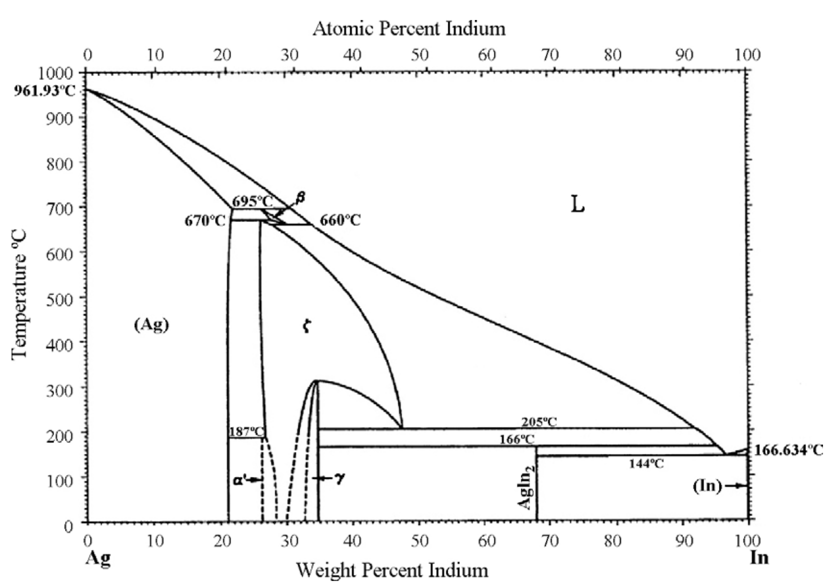

Fig. 1. The In–Ag phase diagram.