Available online at www.sciencedirect.com

ScienceDirect

Sensors and Actuators A 135 (2007) 67–72

SENSORS AND ACTUATORS A PHYSICAL

www.elsevier.com/locate/sna

Thermo-piezoelectric Si_3N_4 cantilever array on CMOS circuit for high density probe-based data storage

Young-Sik Kim[a,*], Seongsoo Jang[a], Caroline Sunyong Lee[b], Won-Hyeog Jin[a], Il-Joo Cho[a], Man-Hyo Ha[a], Hyo-Jin Nam[a], Jong-Uk Bu[a], Sun-Il Chang[c], Euisik Yoon[c]

[a] *Microsystem Group, Device & Materials Laboratory, LG Electronics Institute of Technology, Seoul, Republic of Korea*
[b] *Hanyang Univeristy, Ansan, Republic of Korea*
[c] *University of Minnesota, USA*

Received 1 March 2006; received in revised form 15 September 2006; accepted 5 October 2006

Abstract

A novel wafer level transfer method of silicon nitride cantilever arrays on a conventional CMOS wafer has been developed for the high density usage of probe based data storage device. The cantilevers are so called thermo-piezoelectric cantilevers consist of poly silicon heaters for writing and piezoelectric sensors for reading. The cantilevers were fabricated with a commercial p-type Si wafer instead of a SOI wafer used for this application before. The wafer level transfer method presented here, consists of only one direct bonding of the wafer with cantilevers and the one with CMOS circuits. Thirty-four by thirty-four array of cantilevers were successfully transferred with this method.

With a thermo-piezoelectric silicon nitride cantilever transferred with this method, 65 nm of data bits were recorded on a PMMA film. We also obtained piezo-electric reading signals from the transferred cantilevers.

Keywords: Atomic force microscopy; PZT cantilever; Electrical coupling; High speed; PZT actuator; Piezoresistor; Thermo-piezoelectric cantilever; Wafer-level transfer

1. Introduction

Probe-based data storage devices have been studied extensively to overcome the storage density limits of hard disk drives and semiconductor memories [1–5]. Thermo-piezoelectric read/write mechanism where data bits are written with a resistively heated AFM tip and read with a piezoelectric PZT sensor, was suggested as one of the probe-based data storage devices, as shown in Fig. 1(a) [6–8]. During the write cycle, a resistively heated tip can make indentations on a polymer media and during the read cycle, a piezoelectric sensor detects the indentations from the piezo-electrically generated charges while the cantilever bends over the indentations on the polymer media. The generated charges are amplified and converted to voltage signal by the charge amplifier, as shown in Fig. 1(b).

Thermo-piezoelectrical read/write system has several advantages over the thermo-mechanical read/write system. First, the power consumption is less. In reading, piezo-electrical sensing uses self-generated charges from the cantilever deflection so that power consumption is negligible while thermo-mechanical sensing detects the resistance variation caused by the temperature change of the heated cantilevers, consuming much power. And as the heated cantilevers scan over the polymer media during the reading cycle of the thermo-mechanical system, the media should withstand the heat and this precludes the use of polymers with low glass-transition temperature (T_g), which determines the bit formation temperature as well as the thermal stability of the data bits. The thermo-piezoelectrical system, however, does not have this restriction and can lower the writing power by selecting polymers with low glass-transition temperature.

Second, the electronics is simpler. The thermo-mechanical read system requires additional circuits to compensate the initial resistance difference between cantilevers caused by the process variation. In piezoelectric sensing, such an offset problem does not exist since the initial charge status is all the same for each can-

---

[*] Corresponding author. Tel.: +82 2 526 4582.
E-mail address: ysrevol@lge.com (Y.-S. Kim).

0924-4247/$ – see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2006.10.021

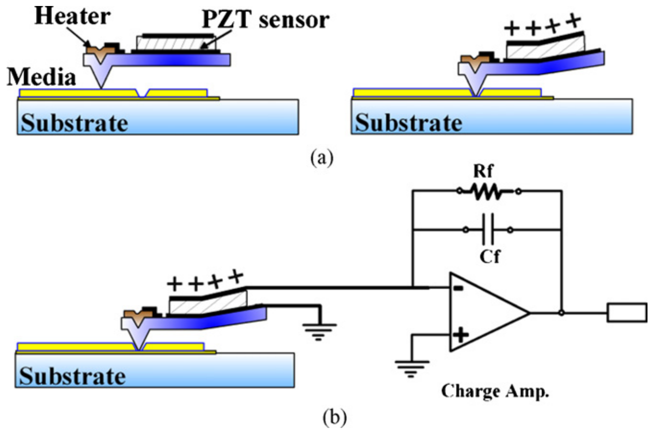

Fig. 1. Principle of PZT sensing of thermo-piezoelectric cantilever: (a) reading mechanism of a thermo-piezoelectric Si_3N_4 cantilever. (b) Self-generated charge in PZT sensor is collected to feedback capacitor (Cf) by charge amplifier and is converted to voltage.

tilever. Finally, the reading speed can be faster with piezoelectric sensor than thermal sensor since the charges are generated within nanoseconds while a few microseconds are needed to heat the cantilever.

A piezoresistive sensor can be another choice, but the sensitivity of the thermal sensor is better than that of the piezoresistive sensor because thermal effects in semiconductors are stronger than strain effects. Vettiger et al. reported that $\Delta R/R$ sensitivity of about $10^{-5}\,\mathrm{nm}^{-1}$ has been achieved with a thermal sensor whereas conventional piezoresistive cantilevers have sensitivity about $10^{-6}\,\mathrm{nm}^{-1}$ [1,2].

For the high density probe-based data storage applications, cantilevers should act in arrays. The cantilevers should be uniform in thickness and stress so that the initial bending and the spring constant of them, which determines the pressing force of the tip on the polymer media, have minimal variation. And the cantilevers can be integrated with ASIC circuit which accesses the individual cantilever for read/write and control. And after the integration of the cantilevers with the ASIC circuit, the tips on the cantilevers can be contacted with the media.

Previously, Vettiger et al. proposed a new micro-device transfer/interconnect method (DTM) compatible with the BEOL CMOS technology. However, this technique consists of two bonding processes; in the first step, cantilevers are formed out of a SOI wafer and the tips are formed on the surface. These cantilevers are transferred onto a glass wafer and the bulk silicon is removed. In the second step, the cantilevers on the glass wafer are transferred onto the CMOS wafer. The SOI wafer is used to control the thickness of the cantilevers [9,10].

The device silicon layer of the commercial SOI wafers has initial thickness variation and this affects the thickness uniformity of the cantilevers. In our previous studies, silicon nitride cantilevers, integrated with heater tips and piezoelectric sensors, were developed with nitride buried SOI wafer. The uniformity of the initial bending and the mechanical stability of the cantilevers can be improved by using the nitride film [7].

In this research, a novel wafer-level transfer method of two-dimensional cantilever arrays on a conventional CMOS circuit has been developed for the high density probe-based data storage devices. The cantilevers and the tips are formed with silicon nitride on a conventional p-type silicon wafer and poly silicon heaters and piezoelectric sensors are integrated with the cantilevers. With one step bonding process, the cantilevers are directly transferred to the CMOS wafer. Our new fabrication process provides simple wafer level transfer method of uniform and mechanically stable cantilever array.

2. Fabrication

Wafer level transfer of cantilever arrays to the CMOS wafer is explained here.

The CMOS wafer consists of arrays of charge amplifier circuits which amplify the signals from the thermo-piezoelectric cantilevers. The wafer was fabricated with 0.8 μm and 2P2M(2-poly-2-metal) process, provided by a standard CMOS foundry in Electronics and Telecommunications Research Institute (ETRI), Korea.

Fig. 2(a) shows the fabricated CMOS wafer by using 0.8 μm conventional CMOS technology. The circuitry for read and write channel per each cantilever are illustrated in Fig. 2(b). The read channel includes a charge amplifier and a latched comparator per one cantilever and the write channel includes a switch transistor per cantilever. The latched comparator converts analog output signals from the charge amplifier to digital output signals and stores the data signals. Using an array of this circuit, fully parallel reading operation can be achieved. The output signal can be acquired from the stored data signals in latched comparators by a column time-multiplexed addressing scheme similar to those implemented in DRAMs.

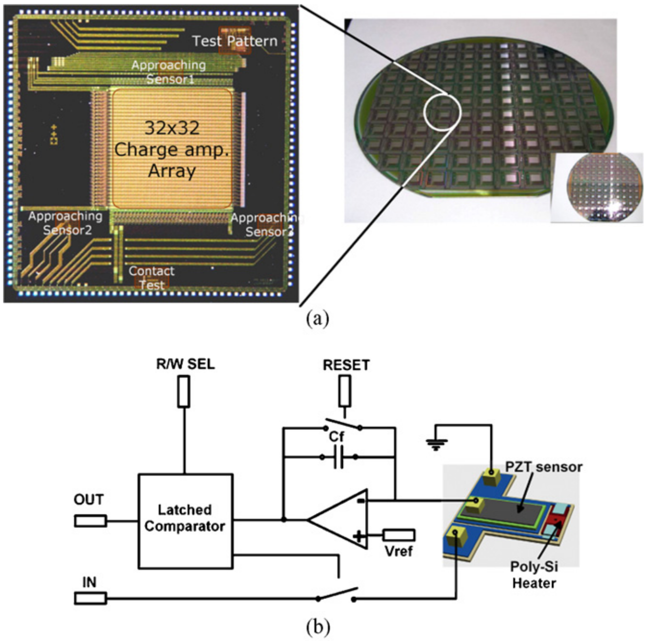

Fig. 2. The fabricated CMOS wafer with Charge amplifier circuitry (a) microscope image of 32 × 32 cantilever array fabricated in 5 in. wafer. (b) Block diagram of read/write circuit per one cantilever.