Sensors and Actuators A 215 (2014) 44–50

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

Design and characterization of micromachined sensor array integrated with CMOS based optical readout

Refik Burak Erarslan[a], Ulas Adiyan[a,*], Sevil Zeynep Lulec[a], Selim Olcer[a], Yuksel Temiz[b], Yusuf Leblebici[b], Hamdi Torun[c], Hakan Urey[a]

[a] Koc University, Electrical and Electronics Eng. Dept, Istanbul, Turkey
[b] Ecole Polytechnique Fédérale de Lausanne, Switzerland
[c] Boğaziçi University, Turkey

ARTICLE INFO

Article history:
Received 19 April 2013
Received in revised form 13 October 2013
Accepted 14 October 2013
Available online 28 October 2013

Keywords:
Thermal detector
MEMS & CMOS integration
Optical readout
Diffraction grating
Fourier optics

ABSTRACT

This paper reports a micro electro-mechanical system (MEMS) based sensor array integrated with CMOS-based optical readout. The integrated architecture has several unique features. MEMS devices are passive and there are no electrical connections to the MEMS sensor array. Thus, the architecture is scalable to large array formats for parallel measurement applications and can even be made as a disposable cartridge in the future using self-aligning features. A CMOS-based readout integrated circuit (ROIC) is integrated to the MEMS chip. Via holes are defined on ROIC by customized post-processing and MEMS chip is thinned down by a grinding process to enable integrated optical readout. A diffraction grating interferometer-based optical readout is realized by pixel-level illumination of the MEMS chip through the via holes and by capturing the reflected light using a photodetector array on the CMOS chip. A model for the optical readout principle has been developed using Fourier optics.

1. Introduction

Integration of MEMS devices with CMOS electronics in a small package enables many key features such as large array operation, low cost, and better control of environment. Integration of optical MEMS devices with customized CMOS has been demonstrated for optical microphones [1] and accelerometers [2]. These are either single devices or a small array of a few devices. Yet, integration of large devices is still challenging and poses a significant bottleneck for current technology.

This paper reports a MEMS-based sensor array integrated with CMOS-based optical readout [3] as shown in Fig. 1a. The MEMS devices in Fig. 1a are electrically passive and free of electrical connections. This enables large array formation for parallel measurement applications. Furthermore, different passive MEMS chips can be used with the same CMOS chip that allows configuring MEMS chips as disposable cartridges. Besides, MEMS chip can be operated in ambient, vacuum, or aqueous environments. A customized post-processing flow is developed to integrate the MEMS chip with CMOS-based readout integrated circuit. Via holes are defined on ROIC to enable integrated optical readout. The chips are aligned with about 1 μm accuracy using self-alignment marks.

It is possible to design sensors, different sensing modalities, and sensitivities on the same array for various applications. Currently, the sensor platform is optimized for thermal imaging applications. The MEMS devices presented in this paper are suspended membranes connected to a transparent substrate via bimaterial and thermal isolation legs. Bimaterial legs that are made of materials with different coefficients of thermal expansion deflect when exposed to thermal input while thermal isolation legs prevent heat dissipation towards the substrate [4–9]. Mechanical deflection is detected optically with sub-nm precision using a pixel-level diffraction grating interferometer [10–13] as illustrated in Fig. 1b. Light reflects off of the membrane interferes with light reflects off of the diffraction gratings embedded under each device. Since the movable reflector, i.e. the membrane, and the reference reflector, i.e. diffraction grating, lay on the same substrate, the readout beam is immune to environmental vibration.

2. MEMS sensor design

MEMS sensor has seven operational structures: transparent substrate, metal diffraction gratings, membrane, infrared (IR) absorber, bimaterial legs, isolation legs, and top reflector as shown in Fig. 2a. A thin metal layer deposited on top of the membrane is used as the IR absorber. The transparent substrate and diffraction gratings are not labeled in the figure since these structures are below the membrane. Incident IR radiation is absorbed by a thin film metal lying on

* Corresponding author. Tel.: +90 212 338 1772.
E-mail address: uladiyan@ku.edu.tr (U. Adiyan).

0924-4247/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.sna.2013.10.014

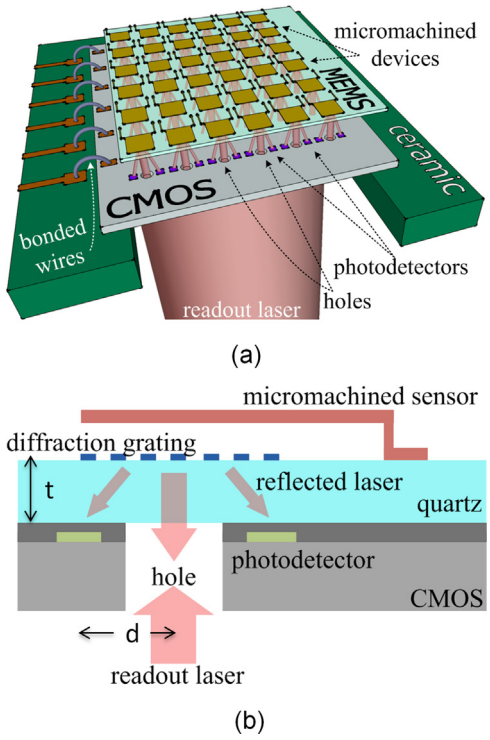

Fig. 1. (a) Side view of one sensor. (b) Schematic of the integrated device.

top of the suspended membrane. Induced temperature load due to absorbed radiation bends the bimaterial legs, which are composed of two materials with different coefficients of thermal expansion. Bimaterial legs are connected to the substrate through isolation legs that provides thermal isolation. Bending on bimaterial legs modulates the gap height between the substrate and the detector membrane. The change in gap is detected by optical means a diffraction grating based interferometer. These structures are illuminated using a laser beam from backside through the transparent substrate as shown in Fig. 1b. The reflected light goes into diffraction orders determined by the diffraction grating. The intensity of light in diffraction orders is modulated by the gap due to interference. The intensity of 1st diffraction order is monitored using a detector located under each MEMS device. Thus, a thermal map of the target is generated. Fig. 2b shows microscope image of individual devices with thicknesses of 400 nm parylene and 200 nm titanium.

The pixels are 35 μm in pitch, and the bimaterial legs of the pixels are 25 μm in length for each side of the pixel. The arrays are fabricated in 64 × 64 array format.The structures are fabricated on a pyrex wafer using a four-mask process. Parylene provides a compliant mechanical support layer and is a good thermal isolator. The CTE (coefficient of thermal expansion) of the parylene is $35 \times 10^{-6}\,K^{-1}$ and the CTE of the titanium is $8.6 \times 10^{-6}\,K^{-1}$ [9]. Therefore, bimaterial legs are made of a combination of parylene with titanium that forms a good thermal mismatch pair. Reflector at the top of the body is made of titanium, patterned with the same mask. The fabrication steps of the parylene/titanium sensor arrays are given in Fig. 3.

Fabrication process is summarized in seven steps. In the 1st step, 100 nm of titanium layer is patterned as diffraction gratings on a pyrex wafer by using lift-off process. In the 2nd step, after coating the photoresist as a sacrificial layer, a photolithography step was performed to define the anchors. After defining the anchors, parylene C is deposited onto wafers as the structural material as a 3rd step. 4th step includes the deposition and patterning of titanium. In the 5th step etching of the parylene layer to define the isolation legs and absorption pads is performed. Release with resist remover and critical point dryer is the 6th step of the fabrication. Lastly, a titanium thin film is deposited as the absorber layer. The MEMS devices given in Fig. 2 are fabricated successfully according to the given fabrication steps.

3. CMOS-based optical readout

Deflection of individual devices in the array is measured using optical methods. Optical readout eliminates the need of electrical interconnects on pixels. So, the devices are free of detrimental effects of joule heating due to electrical bias and thermal crosstalk. Moreover, optical readout improves the sensitivity as it offers sub-nanometer resolution for the detection of the deflection of individual pixels simultaneously. Pixel-level interferometers are formed by blanket illumination of the entire focal plane array (FPA) using a single laser source. Reflected light from the individual devices that propagates in first diffraction order is imaged onto a 2D visible detector array.

3.1. CMOS characterization and post-processing

MEMS chip is integrated with a compatible CMOS ROIC chip to develop a compact and optimized sensing platform. CMOS chip including low power trans-impedance amplifiers, noise cancellation circuits, analog multiplexers, and decoders is designed and fabricated using a standard 0.18 μm CMOS process. Fig. 4 shows ROIC chip that contains an array of holes and photodiodes to be aligned with MEMS devices. The orange box in Fig. 4 illustrates single pixel readout part of CMOS ROIC that includes one hole for

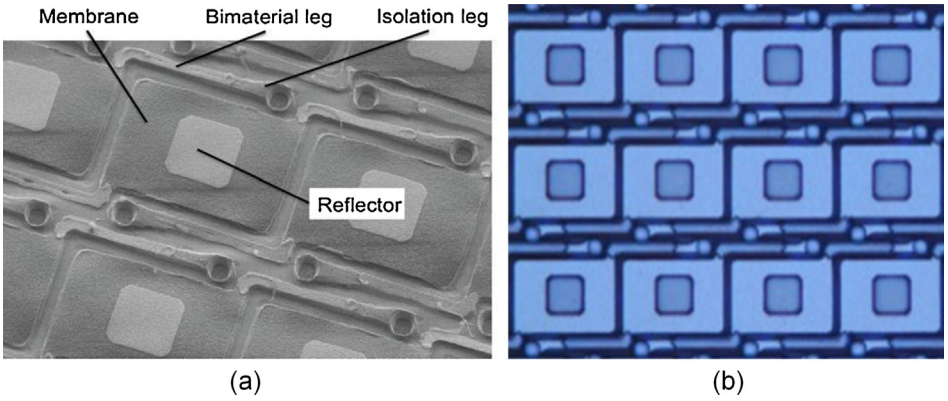

Fig. 2. (a) SEM pictures of 35 μm × 35 μm MEMS sensors. (b) Microscope image of a larger array.