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Single-step deep reactive ion etching of ultra-deep silicon cavities with smooth sidewalls

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ABSTRACT

A process based on deep reactive ion etching (DRIE) has been developed and optimized for the fabrication of millimeter deep silicon cavities with smooth sidewalls. The process combines two approaches which involve an optimized etching process based on the classical Bosch process (Alcatel A601E equipment) followed by the use of an aqueous etchant solution of potassium hydroxide (KOH) to smooth the surface and remove the fluorocarbon contaminants remaining after the DRIE process. As DRIE highly depends on the opening size of the patterned etch mask, different opening sizes have been tested to completely etch through a 1.4 mm thick silicon wafer. Additionally, the effect of different etch-stop materials onto the sidewalls quality has also been characterized. Sidewall quality of etched-through cavities was characterized by scanning electron microscopy (SEM) and contact surface profilometry. This single-step DRIE etching followed by short exposure to KOH solution permits to smooth sidewalls and achieve a surface roughness as low as 50 nm, which is the roughness typically obtained with the Bosch process on standard depths.

1. Introduction

During last few decades, silicon etching has been extensively used in the semiconductor industry. Formerly, wet etching using liquid-phase chemicals such as potassium hydroxide (KOH) was one of the main solutions for silicon etching. However, due to its orientation dependent anisotropic etching, it remained inconvenient for applications requiring high aspect ratios. In the early nineties, plasma etching, mixing passivation and etching steps, was then proposed [1], followed by the invention of the Bosch process [2] which has become one of the most important technologies in modern processes [3]. This technology has since been used to fabricate various micro-systems, such as surface micro-machined gyroscope, accelerometer, pressure and thermal sensors [4], with etch depths extending from a few microns to several tens of microns. The range of applications of deep reactive ion etching (DRIE) has now extended further with the realization of silicon resonator [5], silicon molds [6], diffraction gratings [7,8] and silicon nanopillars [9]. Cryogenic etching is an attractive alternative to the Bosch process. Its ability to obtain smooth and controlled etch profiles along with its high selectivity makes it a very good candidate for etching high aspect ratio cavities [10]. However, because of the complex reactor hardware required to cool the wafer down to temperatures as low as −100 °C, this technique is not widely spread and the Bosch process is often preferred, especially in the industry [3].

As the fabrication of millimeter-scale systems is turning toward micro-fabrication techniques, the need for anisotropic etching with even larger depths is brought forth. For instance, the realization of through-silicon vias (TSVs) for interconnections in 3D packaging applications requires etching of thick silicon wafers while achieving smooth and highly vertical sidewalls [11–14]. Nevertheless, in these cases, DRIE was never performed for depths larger than 500 μm.

Another example concerns the realization of alkali vapor cells for micro-atomic clocks, where DRIE process needs to be optimized for etching down to 1 mm. The process reported in this paper was specifically developed for the fabrication of such alkali vapor cells [15,16]. The latter are typically made of a silicon wafer sandwiched between two borosilicate glass wafers. The cell contains two TSVs, connected through surface micro-channels: one for optical detection and the other for storing an alkali dispenser. Fig. 1 illustrates the structure of such an alkali vapor micro-cell. The aim is to generate these cavities and channels in silicon during a single DRIE process. However, for the application of MEMS atomic clock, the depth of cavities for optical probing plays an important role to determine the short-term clock relative frequency stability. For example, cavity depths of at least 1 mm have been used [17,18].

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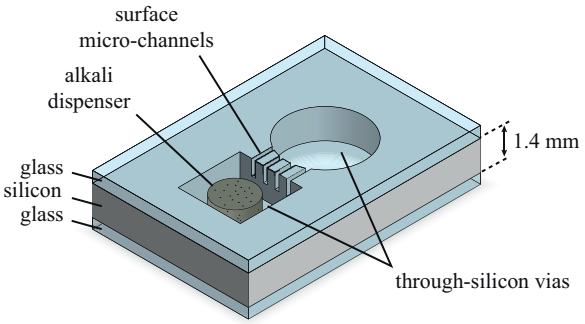

Fig. 1. Schematic of alkali vapor cell for micro-atomic clocks.

In our case we fixed the cavity depth to 1.4 mm. Although there are techniques other than DRIE which have been used to generate TSVs such as, e.g., wet anisotropic etching using KOH [19] or laser drilling process [20], the related processes are either not adapted for vertical etched profile control or time consuming when it comes to generate TSVs with smooth sidewalls. For these reasons, DRIE appears as a good candidate in order to fabricate TSVs, thanks to its good process controllability.

At standard depths ($\leq$100 μm), it is now agreed that DRIE can provide excellent quality sidewalls with roughness as low as a few tens of nanometers [4,6]. However, at millimeter-scale depths, the result is challenged by the formation of grass on the lower part of sidewalls [21]. This is not acceptable in the case of alkali vapor cells used for MEMS atomic clocks where surface roughness can affect the performance of cells in several respects. First, minimizing the area of the internal surfaces can help reducing the amount of cesium consumed during the passivation of the internal surfaces. Residual gases which can be desorbed from surfaces [22] are minimized for the same reason. Finally, when antirelaxtion coatings are used, surface roughness should be as low as possible to avoid imperfection in the formation of the coating [23].

In addition, Aspect Ratio Dependent Etching (ARDE) among structures of different dimensions is exacerbated. Scalloping, a periodic corrugation formed on the sidewalls caused by the etching-deposition cycles, is a well-known problem for features as small as a few hundred nanometers. However, in structures deeper than a few tens to hundreds of micrometers, surface roughening due to the formation of grass, which is caused by micro-masking resulting from the deposition of SiO_2 or resist residues, is predominant [4]. Micro-masking can be due to insufficient etching radicals during the etching step or an excessively long passivation step. During the optimization of the process, a trade-off has to be found and parameters such as selectivity, process temperature, ARDE, notching effects and mask design must also be taken into account.

There have been many studies of these phenomena, however they were limited to depths down to 500 μm [13,6,21,24,25]. In this paper, we investigate DRIE process for structures deeper than 1 mm for which one-step TSVs etching is proposed. Indeed, the fact that a large mask opening is etched faster than smaller features can usually be either an advantage or a disadvantage purely depending on application [13,26]. In our case, the design reported here (Fig. 1) takes advantage of this phenomenon to etch both through-wafer 1.4 mm deep cavities and shallower surface micro-channels in a single step of DRIE. In case of the cell shown in Fig. 1, where two cavities need to be etched-through, surface channels are patterned to let alkali atoms migrate from one cavity to the other once they are generated from a dispenser stored in one of the two cavities. Obviously, such channels cannot be etched-through since the bonding of glass substrates is performed afterward.

Consequently, this paper presents the optimization of DRIE process to fabricate the 1.4 mm TSVs, with highly vertical and smooth sidewalls. Several experiments have been performed in order to achieve TSVs with high quality sidewalls. The paper is organized as follows. In Section 2, we describe DRIE optimization experiments. In particular, the optimization of the process temperature, the etch-stop material, the KOH post-treatment and the mask design are studied. It has to be mentioned that in the specific case of alkali vapor cells, contaminants resulting from the fluorocarbon passivation layers of DRIE can also react with alkali metals and form unwanted alkali fluorides. The latter are expected to degrade the quality of the cell atmosphere. Therefore, the polishing procedure also provides the benefit of removing those contaminants from the surface of the sidewalls. Section 3 describes the generation of surface channels in a single step, along with TSVs. ARDE is therefore characterized in order to control the depth of those channels. Finally, Section 4 discusses the quality of the final TSVs resulting from this process optimization.

2. Experimental optimizations and realizations

In the following, 1.4 mm thick, 4 in. diameter, p-type, (1 0 0)-oriented silicon wafers are considered. DRIE Bosch process is performed with an Alcatel A601E equipment. In order to get highly vertical sidewalls with constant etch rate for the specific structure, etching sequence consists in a polymerization step using C_4F_8 (150 sccm during 3 s) followed by an etching step of SF_6 (300 sccm during 7 s) [27,28]. In addition, to avoid notching (over-etching because of ion attack toward walls at high frequency) at dielectric interface, a low-frequency substrate bias (80 W) is used [5,27] whereas ICP source power is fixed at 1500 W. It must be noted that parameters defined here will be the same for all following experiments.

2.1. Process temperature optimization concept

Several parameters including etch rate, selectivity and etch profile depend on substrate temperature during etching [4,13]. Due to the ion bombardment, local temperature at silicon trenches increases, altering the absorption of ions and changing the thickness of passivation layer. Such changes can be responsible for variations of the etched profile [29]. Thus, the optimal temperature varies with the required etch depth. In this work, we optimized the process temperature for the patterns displayed in Fig. 1. For this purpose, the impact of process temperature on the appearance of grass onto the sidewalls and on the endurance of the resist

Table 1
DRIE process temperatures and resist thickness.

Process temperature		−5 °C	0 °C	5 °C	10 °C	15 °C
Grass appearance		Grass deposition	Grass deposition	Grass deposition	Grass deposition after 2 h 20 min	Excessive grass
Resist endurance	10 μm thick resist	Survived	Survived	Survived	Removed after silicon etching of 1 mm	Damaged
	30 μm thick resist	Survived	Survived	Survived	Survived	Significantly damaged after 20 min