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A Subranging-Based Non-Uniform Sampling ADC with Sampling Event Filtering

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***Abstract*—We propose a two-stage subranging-based non-uniform sampling (NUS) analog-to-digital converter (ADC) that preserves alias-free sampling and improves the effective voltage quantization resolution given the same number of comparators. The subranging architecture divides comparators into two stages (coarse and fine); the voltage reference levels of the fine stage are inserted between the coarse voltage reference levels in proximity to the input signal. A time-out mechanism is used to filter out portions of non-uniformly sampled events while minimizing the impact on the fidelity of the reconstructed signal. A 65nm CMOS prototype implements 15- and 3-level voltage quantizers in the coarse and fine stages, respectively, and achieves a spurious-free dynamic range (SFDR) > 77 dB, an improvement of more than 15-dB compared to an 18-level flash-based NUS ADC with the same average sampling rate. The proposed architecture also reduces the hardware and the number of non-uniform samples by more than 2× when a flash-based NUS ADC architecture is utilized for the same effective voltage quantization resolution.**

***Index Terms*—ADC, alias-free, event-driven, level-crossing, non-uniform sampling, subranging, flash.**

I. Introduction

A flash-based non-uniform sampling (NUS) analog-to-digital converter (ADC) architecture that enables digital anti-aliasing filtering (DAAF) was previously proposed in [1] and implemented in [2]. The unique property of this ADC architecture is that the non-uniformly sampled signal does not cause spectral aliasing, hence allowing error-free signal reconstruction as long as the average sampling rate ($f_{s,avg}$) meets the Nyquist rate of the input signal [3]. Therefore, it can achieve a better signal-to-noise ratio compared to conventional Nyquist rate ADCs with same number of bits in the voltage quantizer [1]. Moreover, since the DAAF can attenuate unwanted out-of-band signals, the burden of anti-aliasing filtering can be moved to the digital domain, which relaxes requirements on the analog anti-aliasing filter and leads to a highly flexible system as the computation can be easily reconfigured [2]. One possible realization of a non-uniform sampler is to generate a sample whenever an input signal crosses a certain voltage level, known as level-crossing sampling [4]. It is completely event-driven and makes the sampling more efficient, especially in applications such as sensor networks and biomedical electronics where signals are often sparse in time. The time instants of sampling are further recorded and quantized. This hybrid quantization strategy that includes both the voltage and time domains favors scaled technology that provides faster device speed.

When a higher voltage resolution is demanded given the same signal reconstruction method, the flash-based NUS ADC requires an increasing number of voltage reference levels (N_{flash}), i.e., comparators. Furthermore, $f_{s,avg}$ increases proportionally with N_{flash} because finer voltage reference levels trigger more signal-crossing activities. In many cases, it is not desirable to couple $f_{s,avg}$ with the voltage quantization resolution. It can cause unnecessary area and power consumption for both analog and digital circuitry, resulting in inefficient implementation for higher resolution.

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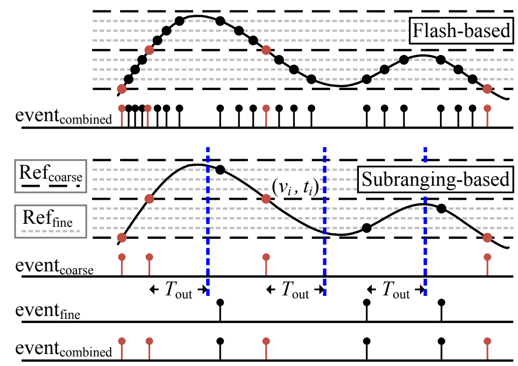

Fig. 1. The proposed subranging-based vs. flash-based NUS ADC.

To alleviate flash-based architecture limitations, we propose a two-stage subranging-based NUS ADC that (a) preserves the alias-free sampling property, (b) maintains the same number of comparators but increases the effective voltage quantization resolution, or reduces the required number of comparators but keeps the same effective quantization resolution, and (c) further reduces $f_{s,avg}$ with minimum impact on the quality of the reconstructed signal. To achieve those goals, we divide the comparators into coarse and fine stages, controlled by the proposed switching scheme, where the voltage reference levels of the fine stage (Ref$_{fine}$) are continuously switched between coarse voltage reference levels (Ref$_{coarse}$) according to the input signal. This not only avoids a dedicated comparator for each Ref$_{fine}$ but also preserves the alias-free sampling. However, $f_{s,avg}$ still increases with increased number of voltage reference levels. Therefore, we propose a time-out mechanism for sampling event filtering. In other words, we can arbitrarily adjust $f_{s,avg}$ based on the need, decoupling it from the voltage quantization resolution.

II. Proposed Subranging-Based NUS ADC

A. Concept

The time-domain view of the proposed subranging-based NUS with time-out mechanism is shown in Fig. 1. If a flash-based NUS is used, one comparator is required for each voltage reference level, resulting in N_{flash} comparators in the voltage quantizer. To reduce the total number of comparators, we switch Ref$_{fine}$ between Ref$_{coarse}$, which results in $N_{coarse} + N_{fine} < N_{flsah}$, where N_{coarse} is the number of Ref$_{coarse}$ and N_{fine} is the number of Ref$_{fine}$ between Ref$_{coarse}$. Unlike a conventional subranging ADC, where a finer voltage quantization resolution is applied on the same sampled input, the proposed

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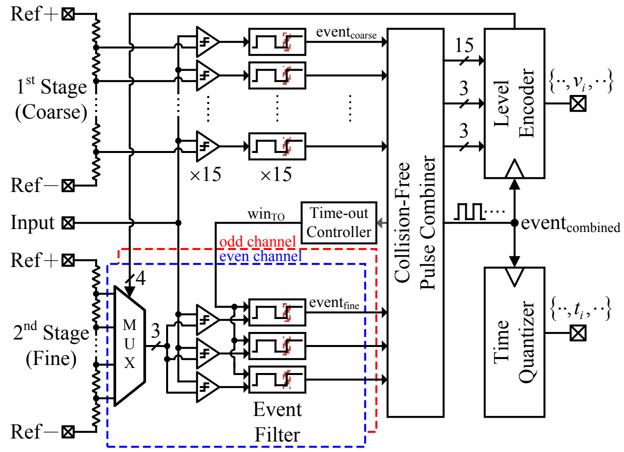

Fig. 2. The block diagram of the proposed subranging-based NUS ADC.

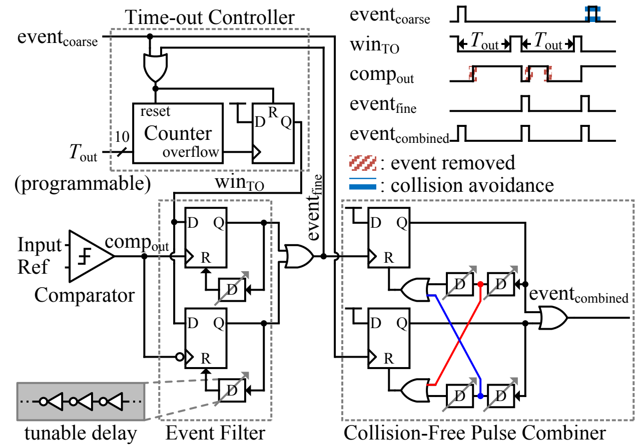

Fig. 3. The circuit implementation of critical building blocks.

architecture generates additional samples from $\mathrm{Ref}_{\mathrm{fine}}$. This fundamentally different operation preserves the alias-free sampling property. Note that, since the extra non-uniform samples may not effectively improve the quality of signal reconstruction, especially when the input signal changes rapidly [5]–[7], i.e., in the high slew rate region, we propose a time-out mechanism that allows new samples to be generated only after a certain time-out duration, T_{out} in Fig.1. Each new level-crossing event re-initiates the time-out mechanism immediately. It thus filters out more non-uniform samples when the input slew rate is higher, and vice versa, resulting in a more efficient distribution of the non-uniform samples. Additionally, by adjusting the value of T_{out}, one can control $f_{\mathrm{s,avg}}$ of this subranging-based NUS, regardless of the number of $\mathrm{Ref}_{\mathrm{fine}}$. It provides the freedom to adjust the overall voltage quantization resolution and $f_{\mathrm{s,avg}}$ independently, which is not feasible for flash-based NUS ADCs.

B. Architecture Implementation

Fig. 2 shows the simplified block diagram of the proposed ADC. The input signal is continuously compared in two stages: the first stage is composed of 15 continuous-time comparators connected with fixed $\mathrm{Ref}_{\mathrm{coarse}}$. The second stage consists of two banks of three comparators (an even and an odd channel) connected to alternating $\mathrm{Ref}_{\mathrm{fine}}$. It can thus track the input signal even when its direction changes immediately after the level-crossing event. Compared to a flash-based NUS ADC with the same quantization resolution, the proposed subranging-based architecture uses only 21 comparators instead of 63, a hardware savings of more than 60%.

After level-crossing events, i.e., transitions at comparator outputs, are generated, they are processed by the event filter. An active-low mask-out window, $\mathrm{win}_{\mathrm{TO}}$, is used to determine whether the events should be removed or converted into pulses ($\mathrm{event}_{\mathrm{coarse}}$ and $\mathrm{event}_{\mathrm{fine}}$). To match the propagation delay between two stages, the event filters inserted in the first stage are replicas of the one in the second stage but with the event-filtering function disabled.

Due to the asynchronous operation between first and second stage, pulses can be corrupted in the pulse-combining process. For example, if an OR gate is used to combine the pulses, adjacent pulses that are too close together will be merged into a wider pulse or will generate glitches, which can affect the operation of the time quantizer [2]. Therefore, a collision-free pulse combiner is proposed to guarantee a properly combined pulse train. Next, the level encoder uses 15 separated pulses from the 1st stage to determine which $\mathrm{Ref}_{\mathrm{coarse}}$ the input signal have just crossed. It can thus still correctly switch $\mathrm{Ref}_{\mathrm{fine}}$ even when any pulses are removed in the pulse combiner. Finally, the time quantizer provides quantized time information at the rising edge of each pulse with a resolution of <9 ps.

III. Circuit Implementation

Implementations of several key building blocks are shown in Fig. 3. The event filter consists of two D flip-flops (DFFs) to detect transitions generated at the comparator output whenever the input crosses the voltage reference level. The time-out controller is mainly composed of a counter, which asserts $\mathrm{win}_{\mathrm{TO}}$ until it reaches the pre-programmed threshold, i.e., T_{out}. T_{out} ranges between 0.5 ns and 500 ns determined by the targeted $f_{\mathrm{s,avg}}$ and the characteristics of input, e.g., signal bandwidth. When $\mathrm{win}_{\mathrm{TO}}$ is high, the transition at DFF input will assert Q at the output to reset the counter and $\mathrm{win}_{\mathrm{TO}}$ to filter the following transitions. After the tunable delay D, Q will be reset, which results in a pulse with width D and releases the reset of the counter to resume counting. In addition to performing event filtering, the event filter can prevent pulses from being closer than $2D$ alleviating the issue of multiple close pulses due to comparator noise, which can cause a malfunction in the time quantizer. D can be determined by the design of time quantizer, which is ~250 ps in this prototype. Finally, the collision-free pulse combiner contains a cross-coupled reset path. When a pulse is detected from either the first or second stage, it will block the following incoming pulses if they are too close together and thus prone to collisions or glitches.

Whenever the input crosses a new $\mathrm{Ref}_{\mathrm{coarse}}$, $\mathrm{Ref}_{\mathrm{fine}}$ are switched accordingly. However, the input signal may change its direction immediately and cross the same $\mathrm{Ref}_{\mathrm{coarse}}$ again. It can impose a stringent settling requirement on $\mathrm{Ref}_{\mathrm{fine}}$. Therefore, we propose an alternating switching scheme shown in Fig. 4. The even and odd channels are responsible for monitoring level-crossing events from different intervals between $\mathrm{Ref}_{\mathrm{coarse}}$. However, only the channel, which is farther from the input signal, switches at each level-crossing event. $\mathrm{Ref}_{\mathrm{fine}}$ are derived from the resistor ladder and multiplexed via an array of thick-oxide devices to minimize the input-dependent leakage current. Because comparators in the 1st stage are connected to fixed voltage reference levels, the overall ADC throughput will not be limited by the settling of the fine voltage reference levels.

The comparator implementation (Fig. 5) consists of multi-stage pre-amps followed by a differential-to-single-end converter. Due to finite gain and bandwidth, the comparator can generate an input slew rate dependent propagation delay, which can cause distortion at the output. To minimize the impact, comparators are designed with more than 60 dB overall gain and 1 GHz bandwidth for each stage according to the analysis in [2]. To relax the matching requirements between comparators, the offset calibration routine is accomplished in two