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Electronic monitoring of single cell-substrate adhesion events with quasi-planar field-effect transistors

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ABSTRACT

In the present study, we investigate the applicability of open-gate silicon field-effect transistors (FET) with a quasi-planar topography for Electrical Cell-substrate Impedance Sensing (ECIS) of individual cells. These newly developed chips have a thinner gate oxide layer leading to higher transconductance values and therefore to a stronger electrical coupling between the cells and the transistor gates.

Three histologically different cell lines were cultivated the FET devices and subjected to microscopic analysis of gate coverage and electrical measurement of cell adhesion. The used measurement technique, called transistor-transfer function (TTF) sensing, is comparable to the well-established ECIS method. The different morphologies of the tested cells resulted in different frequency spectra recorded by the presented method. With our TTF method we are able to extract cell-related parameters such as seal resistance and membrane capacitance from the measured spectra using an equivalent electrical circuit model. The results of our study demonstrate the reliability of the newly developed planar FETs and implicate the applicability of our system to be used as a pharmacological platform for studying the effects of chemical and therapeutic compounds on a variety of cells coming from different histological backgrounds.

1. Introduction

Silicon-based field-effect devices have become progressively more important in the research field of biosensors and were successfully used for several applications like antigen detection [1], DNA detection [2] or cell adhesion studies [3,4]. An especially promising type of device with diverse applications ranging from cytotoxicity analysis [5] to pharmacological assays for the development of new chemotherapeutic compounds [6] are field-effect transistors (FETs). Development of new anti-cancer compounds is a costly and time consuming process, therefore, high throughput platforms for pharmacological testing are needed. In addition to having the properties of user-friendliness and simultaneous multiple readout capability, such platforms need to be flexible to work with a wide variety of biological samples. Especially for the development of antineoplastic drugs, it is of utmost importance to provide a system that can handle a wide range of cells in different morphologies in order to establish testing regiments for histologically different cancer types. In this work we show the ability of our already established FET system to handle morphologically different cell types reaching down to the single cell level.

In addition to already established platforms like the Electric Cell-substrate Impedance Sensing system (ECIS) [7], the main advantages of ion-sensitive FETs are their high sensitivity to surface potential changes at the liquid-solid interface, their high potential for miniaturization, a high level of reusability and the possibility to analyze pH changes affecting adhering cells. FETs can be downscaled to such a small sensor size that differences of adhesion profiles of single cells can be recorded. The ECIS systems use electrodes ranging in diameter from 25 to 250 μm [8–12] and therefore typically provide data on the collective response of cells to a defined physiological stimulus. However the ECIS technique has its limitations with the lower size limit for metal electrodes in bioimpedance assays being 25 μm in diameter [11], making it difficult to reach single-cell resolution. By utilizing FETs in the size range below 25 μm, reactions to external stimuli can be analyzed on a single cell level. The data obtained from such averaged cell populations might conceal individual reactions associated to the heterogeneous properties of cells [13]. Therefore it should be of interest for certain specific applications to analyze individual cellular reactions rather than obtaining averaged results from cell populations by ECIS.

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In this work we present a newly developed type of ion-sensitive FET with a quasi-planar topography. These devices were developed at our institute and provide several improvements over previous FET types. Simulations done in our group [14] promised an improved electrical performance for these FETs due to their optimized gate dimensions and thinner gate oxide layer leading to higher transconductance (g_m) values. In addition their quasi-planar surface is leading to a stronger electrical coupling between cells and transistor gates, thereby resulting in a higher sensitivity of the sensors. The experiments conducted during this work are aimed at showing the benefits provided by these new chips in cell culture analysis. The method of analysis used in this publication is based on the recording of the transistor-transfer function (TTF) [15–17]. Using our custom-build FETs, we are able to provide data concerning the reactions of both confluent cell layers and of single cells to external stimuli (e.g. drug application) by utilizing transistor gates in sizes typically smaller than the adhesion footprint of a single cell (with a width of 12–25 μm and an electrically active length of 1–2 μm). Using an electrically equivalent circuit (based on the point-contact model) to describe a transistor in contact with an adhered cell, we can analyze parameters like the seal resistance (R_{seal}) or combined membrane capacitance (C_M) giving us a deeper insight into cellular reactions to external stimuli [14]. This approach can be employed for adhering cell types coming from different histological backgrounds, thereby substantiating the systems applicability in cancer research and pharmacological research.

2. Materials and methods

2.1. Fabrication of quasi-planar FETs

The process flow of the FET devices, which were fabricated for this study, is presented in Fig. 1. Compared to previously published protocols for our p-type open-gate FETs [18,19], the process for quasi-planar devices included only four optical lithographies. We use implanted contact lines for this design, although this typically results in large feed line resistances and capacitances. However, by this design we end up in moderate frequency ranges for the observed cell impedance profiles (typically in the range of 10 kHz–1 MHz) and most importantly to an enhanced robustness of our FET devices, which are reusable for many times of cell cultures.

The fabrication of the devices was done on n-type silicon wafers (4 in. resistivity 2–10 Ω cm, Si-mat, Germany). In the first step, 1 μm silicon oxide was thermally grown in a wet oxidation process (1000 °C, 5 h), which acted as the masking layer for the ion implantation process. Prior to the oxidation, the wafers were cleaned by a standard RCA (Radio Cooperation of America) protocol. The contact lines were defined by optical lithography and wet etching of silicon oxide by buffered hydrofluoric acid (BHF). The photoresist was removed and the wafer was cleaned by a standard RCA protocol before the first ion implantation. To reduce the contact line resistances, boron ions were implanted with a high dose and energy (1×10^{16} ions/cm^2, 150 keV) by an external supplier (IPS, France). The wafers were then cleaned in piranha solution with 1% hydrofluoric acid (HF) and annealed at 1050 °C for 2 h to activate the boron ions. We defined the source and drain electrode areas by a second optical lithography and subsequent wet etching of the silicon oxide by BHF. A second boron implantation was done with a dose of 1×10^{15} ions/cm^2 and an energy of 80 keV. In the next step in order to achieve a quasi-planar topography, all silicon oxide layers were completely removed from the entire wafer by wet etching in BHF and subsequent cleaning by the RCA protocol. Then the wafers were annealed for 10 min in N_2 and subsequently brought into a wet oxidation process for 30 min, both at 900 °C. With this annealing process we aimed to activate the dopants and to achieve a uniform 220 nm thick SiO_2 passivation layer on the complete chip surface. A third lithography was applied to define the gate area and the outer source and drain contacts for final metallization. This etching step is quite delicate, since the surface, where the gate oxide is grown, will be opened. To reduce the roughness created by the wet etching process on the gate areas, the 220 nm thick silicon oxide layer was etched in BHF for 3 min and subsequently in 1% HF until the silicon oxide was totally etched. The resist was removed by acetone only and the wafer was carefully cleaned by an RCA protocol. The gate oxide layer was then thermally grown in a dry oxidation process (820 °C, 40 min), which formed a 6 nm thick silicon oxide as gate dielectrics for the FET devices. At the end of the device fabrication, the outer metallizations to the source and drain contact lines were realized in a lift-off process. Prior to metal evaporation, the silicon oxide on the source and drain contacts were etched by 1% HF. A metal stack of 200 nm of aluminum, 20 nm of titanium and 100 nm of gold was deposited using electron beam evaporation. The metal contacts were then annealed for 10 min at 400 °C in N_2 atmosphere in order to form good ohmic contacts. We used our standard design where transistor gates are arranged in a 4 × 4 pattern localized in the center of a 7 mm × 7 mm chip with a distance of 200 μm between individual gates. Typical gate size was 12 μm × 5 μm (mask design), which resulted in an effective gate length of about 1.3 μm due to under-diffusion in the process described above. Electron microscopy images show the almost planar design (Fig. 2). Only at the gate area an

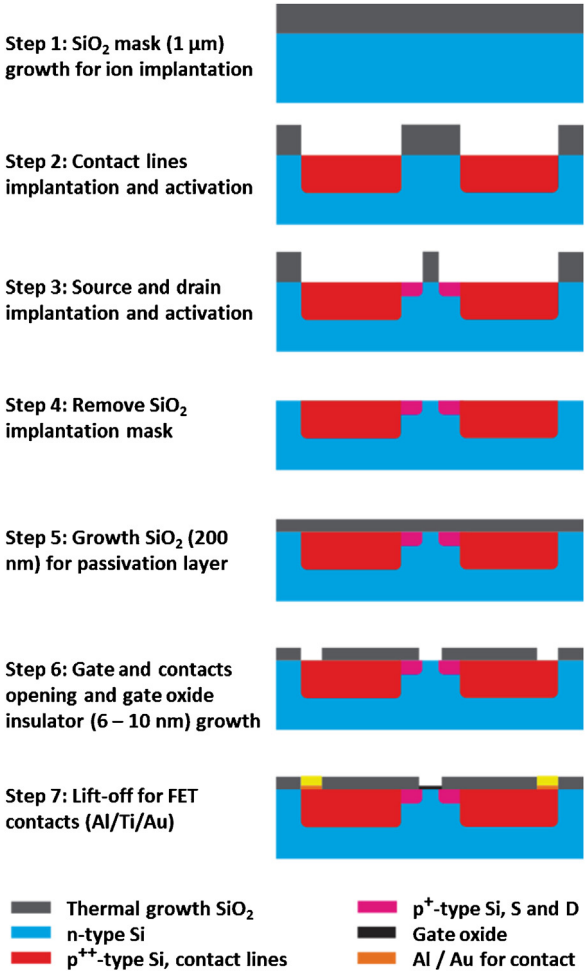

Fig. 1. Process flow for the fabrication of quasi-planar FETs for individual cell adhesion measurements: the individual steps of the protocol are described in detail in the text.