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Sensor system including silicon nanowire ion sensitive FET arrays and CMOS readout

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ABSTRACT

We present a highly sensitive chemical sensor system including a chip with an array of silicon nanowire ISFETs and a CMOS chip with custom-designed signal-conditioning circuitry. The CMOS circuitry, comprising 8 sigma–delta (Σ–Δ) modulators and 8 current-to-frequency converters, has been interfaced to each of the nanowires to apply a constant voltage for measuring the respective current through the nanowire. Each nanowire has a dedicated readout channel, so that no multiplexing is required, which helps to avoid leakage current issues. The analog signal has been digitized on chip and transmitted to a host PC via a FPGA. The system has been successfully fabricated and tested and features, depending on the settings, noise values as low as 8.2 pA_{RMS} and a resolution of 13.3 bits while covering an input current range from 200 pA to 3 μA. The two readout architectures (Σ–Δ and current to frequency) have been compared, and measurements showing the advantages of combining a CMOS readout with silicon nanowire sensors are presented: (1) simultaneous readout of different silicon nanowires for high-temporal-resolution experiments and parallel sensor experiments (results from pH and KCl concentration sweeps are presented); (2) high speed measurements showing how the CMOS chip can enhance the performance of the nanowire sensors by compensating its non-idealities as a consequence of hysteresis.

1. Introduction

Silicon nanowire (SiNW) field effect transistors (FETs) have recently received great attention for their potential with regard to label free detection of biological and chemical species. Owing to their high surface-to-volume ratio and quick response, they are promising candidates for highly sensitive sensors. SiNWs have, for example, been successfully used for the detection of DNA [1], proteins [2], for pH measurements [3], and for recording the activity of electrogenic cells, such as neurons [4].

The detection principle of a SiNW-based sensor is similar to that of an ion sensitive field effect transistor (ISFET), a well-known device first introduced in 1970 by Bergveld [5].

A SiNW FET, as well as an ISFET, can be considered as a normal MOS transistor, whose metallic gate is replaced by a liquid solution and a reference electrode controlling the potential of the liquid. A sketch of such a SiNW FET is shown in Fig. 1a, with its cross section displayed in Fig. 1b (further details will be described in the following sections). The charges coming from, e.g., ions, proteins, DNA, dispersed in the liquid solution accumulate at the surface of the gate oxide on top of the SiNW. This charged layer induces a surface potential change that can modulate the current flowing through the NW, in the same way as a gate voltage modulates the current flowing through the channel of a MOS transistor. The surface potential is therefore depending on the amount of charges in the liquid solution, and thus on the analyte concentration. Since the surface potential is directly affecting the threshold voltage of the transistor, a change in the analyte concentration causes a shift of the threshold voltage: for a p-channel device (having negative threshold voltage), an increase in positive charge on the surface will reduce the threshold voltage and will lead to a decrease in the current flowing through the channel for a defined sensor geometry and defined electrochemical conditions (reference electrode voltage).

An equation showing the relation between surface potential, Ψ, and the threshold voltage, V_{th}, of an ISFET was first introduced in [6]:

$$V_{th} = V_{lg} - \Psi + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{SS} + Q_B}{C_{ox}} + 2\phi_f \quad (1)$$

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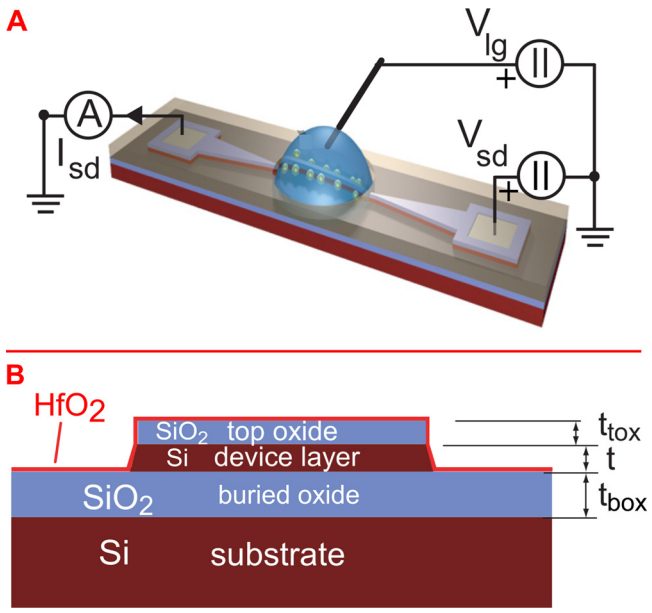

Fig. 1. (a) Sketch of a SiNW FET sensor and its electrical connections: the source–drain voltage (V_{sd}) is clamped, while the current I_{sd} is measured; a voltage V_{lg} is applied to the reference electrode in the liquid solution. (b) Cross section of the SiNW FET sensor including key parameters: buried oxide thickness, t_{box} = 145 nm; silicon device layer, t = 85 nm; top oxide layer, t_{tox} = 15 nm; layer of HfO_2 with thickness of 8 nm.

where V_{lg} is the voltage applied at the reference electrode, χ^{sol} is the surface dipole potential of the solvent, Φ_{Si} is the work function of the silicon; the fifth term represents the charge accumulated in the oxide (Q_{ox}), at the oxide–silicon interface (Q_{SS}) and the depletion charge (Q_B); the last term is an indicator of the onset of inversion depending on the dopant concentration. The parameter χ^{sol} is a parameter of the liquid solution, whereas all the other terms characterize the device itself. The signal that is transduced from the chemical to the electrical domain is represented by changes in Ψ, the surface potential, which – as already mentioned – will directly be detectable as threshold voltage changes (for a given V_{lg}). Even though this physical description was originally developed for ISFETs, it can be also used to describe the behavior of SiNW FETs under certain conditions [7].

One important issue in the design of SiNW FET sensors is an efficient readout of the sensor output signal, which is normally rather weak and noisy. Most of the work cited so far [1–4] focus on the fabrication of the NW sensors and on their use. The measurements have been done by using bulky lab equipments, which, however, can limit the sensor performance.

A better solution is to use readout circuits fabricated in CMOS technology. The main advantage is the possibility of having the sensors and readout as physically close together as possible, potentially even on the same substrate. Moreover, the use of CMOS technology brings other advantages: many sensors can be simultaneously read out in parallel; sensor signals can be digitized right after the measurement to take advantage of the high robustness and flexibility of digital circuits; non-idealities of the sensor can be compensated in order to improve its performance. The CMOS approach is very powerful for integrating NW-based sensors into portable point-of-care devices that, e.g., can simultaneously detect different analytes in a solution or body fluid.

At the circuit level, a common measurement approach for SiNW FET sensors is to keep the voltage across the NW (V_{sd}) constant, to fix the voltage at the reference electrode (V_{lg}), and to measure the current flowing through the device (I_{sd}), as sketched in Fig. 1a. In such configuration, changes in the threshold voltage will directly be detected as changes in the current: the resistance or conductance of the NW is measured.

Extensive work has been done to design CMOS current readout circuits, many of which are not specifically suitable for NW-based sensors. Here we only briefly review some typical architectures.

A well-known challenge in designing CMOS circuits is to find the best trade-off among noise performance, bandwidth, input current range, power consumption and needed silicon real estate. The last two points become especially important for designing readouts for sensor arrays. Meanwhile, the input sensor current range can be quite large (several orders of magnitude, from few hundreds of pA to few μA), and it is, therefore, not easy to realize circuits with extremely low noise (few pA_{RMS} or less) for such wide input current ranges.

A popular current readout circuit architecture is the transimpedance amplifier (TIA), due to its low noise and bandwidth of several kHz that can be achieved (noise of few fA_{RMS} have been reported [8,9]). On the other hand, TIAs can be rather bulky and they also require a dedicated analog-to-digital converter (ADC) to digitize the output voltage resulting from the measured current. Integrated versions of lock-in amplifiers have also been presented [10,11], which provided good noise performance again at the cost of area and complexity.

Other architectures previously used as ISFET readouts include circuits able to directly measure the threshold voltage changes [6] or circuits that incorporate the sensor itself as part of the readout circuit in so-called sensing circuits [12]. These architectures either use complex circuits or are technologically challenging (in terms of monolithic integration) when applied to SiNWs.

For the work presented in this paper we focused on two architectures also widely used in the chemical and bio-sensor field: sigma–delta (Σ–Δ) modulators and current-to-frequency (ItoF) converters. Both topologies have limited bandwidth (only suitable for slow varying signals) but are fast enough for most applications with SiNW sensors. Moreover, Σ–Δ and ItoF converters have the advantage of sensing and digitizing the current at the same time. Σ–Δ modulators have been demonstrated to feature low noise levels and high resolution [13,14], while they have a high degree of complexity and are difficult to design. ItoF converters, on the other hand, are rather simple and scalable circuits and thus suitable for arrays [15]; moreover, they can cover a wide input current range [16,17], while noise levels and resolution are sometimes not as good as those of Σ–Δ topologies.

Most of the cited work describes the CMOS circuits or their use in combination with micro and nano electrode arrays. Only few publications to date reported the integration of a CMOS readout chip and a SiNW sensor array [18–20]. Most of these systems feature one single readout channel that is multiplexed to several NWs [18,20]. The multiplexing approach suffers from leakage currents (up to few pA [18,20]) coming from the switches that have been used to connect each of the NW sensors to the readout circuit; multiplexing also does not allow for a simultaneous readout of different sensors. In addition, previous works [18–20] measure mostly the NW conductance change. Although conductance measurements may be sufficient for most applications, it is important to remember that the characteristic sensing effect in SiNWs is related to the threshold voltage shift. Non-idealities of the SiNW sensor, e.g., hysteresis, may induce unwanted threshold voltage shifts so that measured conductance changes may be caused by irrelevant sensing event.

We present a nanowire sensor system, featuring (i) a CMOS readout chip and a SiNW sensor array; (ii) each NW sensor has a dedicated readout channel; (iii) the CMOS chip includes both Σ–Δ modulators and ItoF converters in order to compare and discuss their performance and potentials as SiNW sensor readout circuits; (iv) simultaneous recordings from several NWs at high temporal resolution and the corresponding statistics are shown; (v) the