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Fabrication and fluidic characterization of silicon micropillar array electrospray ionization chip

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Abstract

A silicon electrospray ionization (ESI) chip for the mass spectrometric analysis is designed, fabricated, and characterized. The chip has three parts: a liquid sample introduction spot, a flow channel, and a sharp electrospray ionization tip. A regular micropillar array is micromachined inside the whole channel. The chip has no lid, which makes the sample application and chip fabrication easier. A two photomask level fabrication process utilizes nested masks of silicon dioxide and aluminum oxide. A combination of anisotropic and isotropic plasma etching steps allows formation of a truly three-dimensional electrospray ionization tip without double-sided lithography. The filling properties of the lidless micropillar channel are studied. Because of the capillary forces facilitated by the micropillar array, the sample applied onto the sample introduction spot spontaneously fills the whole flow channel including the electrospray ionization tip, without external pumping. Besides reliable self-filling, the chip offers stable electrospraying and high sensitivity chemical analysis when coupled to a mass spectrometer (MS).

Keywords: Silicon microfabrication; Electrospray ionization; Mass spectrometry; Microfluidics; Capillary filling; Micropillars

1. Introduction

There is a constant demand for faster, more selective, and more sensitive analysis methods of drug and biomolecules using smaller sample volumes. A microfluidic device coupled to a mass spectrometer (MS) has potential to respond to these demands [1]. Electrospray ionization (ESI) has been the most studied method for miniaturized mass spectrometer interfaces. The most popular fabrication materials of ESI chips have been glass [2,3] and polymers, such as parylene [4], PDMS [5], and SU-8 [6]. However, these materials set limits to chip designs. Glass microfabrication techniques are cumbersome compared to silicon micromachining and through-wafer processing is inaccurate. Polymer microfabrication is generally easy and fast, but at the moment it does not match silicon in fabrication of robust high aspect ratio structures and complex three-dimensional features.

Silicon ESI chips [7–9] have also been realized because of the well-explored microfabrication techniques of silicon. However, the conductivity of silicon limits its use, because it excludes the use of electroosmotic flow in sample transport. Pressure driven flow [2] has been the other popular method used for sample transportation in previous ESI chips. However, both of these methods require an external actuator, such as a high-voltage supply or a pump. Pressure driven flows also require the use of troublesome fluidic connectors. Some ESI chips exploit capillary forces to transport the sample, but narrow or enclosed channels are usually required in order to achieve sufficiently strong capillarity [9,10].

We present a micropillar array electrospray ionization (μPESI) chip, where the liquid sample is transported through

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a 1-mm wide lidless flow channel by capillary forces facilitated by micropillars. No external pumping is required and the only high-voltage source needed is the one necessitated by electrospray ionization and the MS. The whole chip is made of silicon, which allows the fabrication of high aspect ratio micropillars inside the channel. Silicon micromachining makes also possible to accurately define a truly three-dimensional ESI tip, which is in-plane. We investigated how the pillars contribute to capillary filling properties of a lidless channel. The analytical potential of μPESI chip was demonstrated in MS measurements.

2. Device design and fabrication

The μPESI chips were fabricated on 300–μm thick ⟨1 0 0⟩ silicon wafers that had resistivity of 1–50 Ω cm. Both p and n-type wafers were used. The chip has a 2.5-mm wide circular sample introduction spot and a 5.5-mm long and 1-mm wide straight flow channel, which ends to a sharp, in-plane ESI tip. The chip has no lid. Both the sample introduction spot and the flow channel contain a perfectly ordered array of micropillars. Two different sets of geometrical parameters for pillar dimensions and pillar packing were used. The geometrical parameters are presented in Fig. 1. Similar chips without the pillar array were also fabricated for reference. The depth of the channels was varied between 20 and 40 μm. A photograph of a fabricated chip is shown in Fig. 2.

The fabrication process had two mask levels and utilized nested masks of silicon dioxide (SiO_2) and aluminum oxide (Al_2O_3), which were both patterned on the wafer prior to any silicon etching. First, SiO_2 was thermally grown on the wafers. The SiO_2 mask for pillar channels was etched by

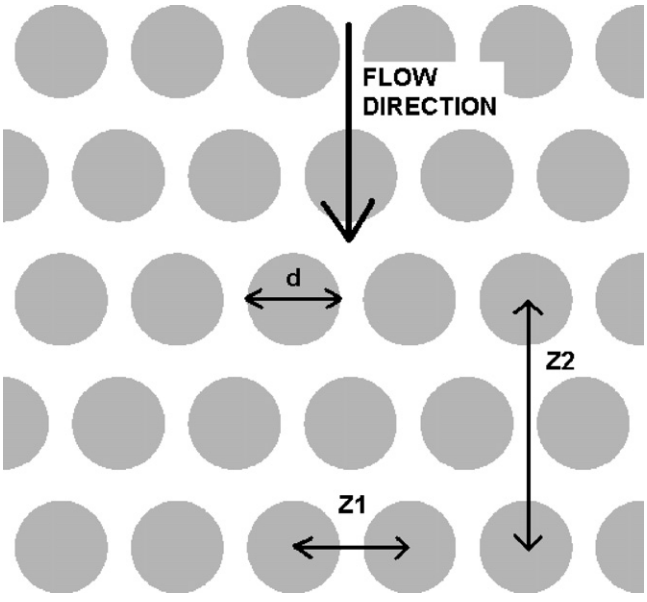

Fig. 1. Packing of the pillars inside the channel. In the first set-up (denser packing) the pillar diameter d was 10 μm and the pillar centre-to-centre distances Z1 and Z2, were 12 and 22 μm, respectively. In the second design d = 60 μm, Z1 = 75 μm and Z2 = 160 μm.

Fig. 2. A μPESI chip on a 10 euro cent coin.

CHF_3/Ar reactive ion etching (RIE) using a photoresist mask (Fig. 3a). After photoresist removal, amorphous Al_2O_3 layer was deposited on top of the patterned SiO_2 mask using atomic layer deposition (ALD). The deposition took place at 220 °C, trimethylaluminum and water vapor being the source gases. The second lithography defined the sharp ESI tip at the end of the flow channel. Both Al_2O_3 and SiO_2 were etched away from tip area, by phosphoric acid and CHF_3/Ar RIE, respectively (Fig. 3b and c). Aluminum oxide served as an etch mask during the through-wafer deep reactive ion etching (DRIE) (Fig. 3d).

If three-dimensionally sharp ESI tip is desired, the through-wafer etching has to be done in two parts. First, fairly shallow anisotropic silicon DRIE step is performed. Then, a 250-nm thick SiO_2 passivation layer is deposited using plasma enhanced chemical vapor deposition (PECVD). Deposited PECVD SiO_2 is removed from horizontal surfaces using CHF_3/Ar RIE again, but vertical sidewalls remain passivated because of the anisotropic nature of the RIE step. The rest of the through-wafer etching is also done with DRIE, but using a more isotropic etching process. Isotropic etching causes undercutting and because of the passivation layer a three-dimensionally sharp tip is formed. The two-step anisotropic–isotropic sharpening process is not shown in Fig. 3.

After the through-wafer etching, the Al_2O_3 mask was removed in phosphoric acid (Fig. 3e) and the pillar channels were created in another anisotropic silicon DRIE step, using the revealed SiO_2 pattern as a mask. All silicon etchings were done in inductively coupled SF_6/O_2 plasma at cryogenic temperature [11] (Plasmalab System 100, Oxford Instruments, UK). After the last silicon DRIE step, the remaining SiO_2 was removed using buffered hydrofluoric acid (Fig. 3f). The channels can be transformed to more hydrophilic using short oxygen plasma treatment or Piranha treatment. Because the channel is lidless, no bonding is required in fabrication process.