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Behavior of subthreshold conduction in junctionless transistors

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ABSTRACT

In this work, the effect of high channel doping concentration and unique structure of junctionless transistors (JLTs) is investigated in the subthreshold conduction regime. Both experimental results and simulation work show that JLTs have reduced portion of the diffusion conduction and lower effective barrier height between source/drain and the silicon channel in subthreshold regime, compared to conventional inversion-mode (IM) transistors. Finally, it leads to a relatively large DIBL value in JLTs, owing to degraded gate controllability on channel region and strong drain bias effect. However, JLTs showed a better immunity against short channel effect in terms of degradation of the effective barrier height value.

1. Introduction

As channel length of devices shrunk extremely, the formation of junction at source and drain side becomes a major challenge because, in few nanometer scale devices, even a small deviation of doping concentration can cause significant variation of device performance. To circumvent the problem, the junctionless transistor (JLT) having single doping concentration from source to drain was suggested and has received huge interest [1–3]. Since the device has single doping concentration in its channel, it has easy fabrication process with low thermal budget for the choice of gate stack as well as unique conduction mechanism [4]. JLTs also have shown excellent immunity to short channel effect and advantages for the mobility by reduced transverse electric field [5–8]. While the conventional inversion-mode (IM) transistor has strong inversion channel at the interface between channel silicon and gate insulator, the junctionless transistor has bulk neutral channel with the gate bias above threshold voltage. Besides on-state conduction, the channel without junction results in distinguished subthreshold behaviors compared to the IM transistor. Although there are reports about SS and DIBL in JLTs so far, its performance regarding SS and DIBL is still debated [3,9–11]. Thus, here is a need to study the relation between subthreshold conduction and channel without S/D junction in detail, according to different doping concentrations and device structures, for a better understanding of DIBL and SS behavior in JLTs.

In this study, it is shown that JLTs have reduced contribution of diffusion conduction in subthreshold operation region through subthreshold slope curve and extracted effective barrier. The reduction of the diffusion conduction is closely related to large DIBL in JLTs, as reported previously [3,9]. Experimental results on subthreshold property of JLTs are also confirmed with 2-D numerical simulation.

2. Experimental details

Fabrication of JLT devices was started with (100) SOI wafers having 145 nm buried oxide thickness at CEA-LETI. After thinning down of the channel silicon to ≈9.4 nm, the channel was doped with phosphorus full-sheet implantation, targeted at $2 \times 10^{19}\,cm^{-3}$ or $1 \times 10^{19}\,cm^{-3}$. As a result, the effective doping concentration was achieved as about $1 \times 10^{19}\,cm^{-3}$ and

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5×10^{18} cm^{-3}, respectively [12]. An additional implantation in S/D regions was carried out with doping concentration of 1×10^{20} cm^{-3}, like IM transistor, to reduce access resistance. The channel of counterpart IM transistor was not intentionally doped. The effective oxide thickness of gate stack (HfSiON/TiN/Polysilicon) reached around 1.2 nm. The mask channel length L_M varied as 50 nm/100 nm/1 μm, to observe subthreshold behavior with channel length variation and the mask channel width W_M was 10 μm for the planar JLT. Nanowire JLT has dimension of L_M = 1 μm and W_M = 80 nm. More details related to the fabrication process and device information have been described in Ref. 13. In addition, 2-D numerical simulation carried out with Poisson equation using Flex PDE 5.0 software based on the finite element method.

3. Results and discussion

3.1. The subthreshold current on JLTs

The subthreshold current in conventional MOSFETs is originated from the thermionic emission over junction barrier, existing between highly doped source/drain region and channel region, and diffusion current from source to drain, in series [14,15]. Due to these reasons, the subthreshold current in IM transistor is exponentially increased with gate bias while the above-threshold drain current of linear operation regime is linearly increased with gate bias. On the other hand, it is expected that JLTs have different subthreshold current behavior from that of IM transistor because of the elimination of source/drain junction and heavily doped channel.

Fig. 1 show the drain current (I_d), slope curve (dLog(I_d)/dV_g) and the derivative of transconductance (dg_m/dV_g) as a function of V_g at V_d = 20 mV in JLTs of two different doping concentrations and IM transistor (L_M = 1 μm, W_M = 10 μm), respectively. From the derivative of transconductance curves, the threshold voltage was determined. The second peak point of dg_m/dV_g plots in Fig. 1 (b) and (d) also represents flat-band voltage (V_{fb}) in JLTs [3]. Highly doped JLT ($N_D = 2 \times 10^{19}$ cm^{-3}) doesn't show a clear linear slope in subthreshold current as illustrated in Fig. 1(a), although subthreshold current of IM device increases with a perfectly linear trend in logarithmic scale as raising V_g, indicating exponential increase of

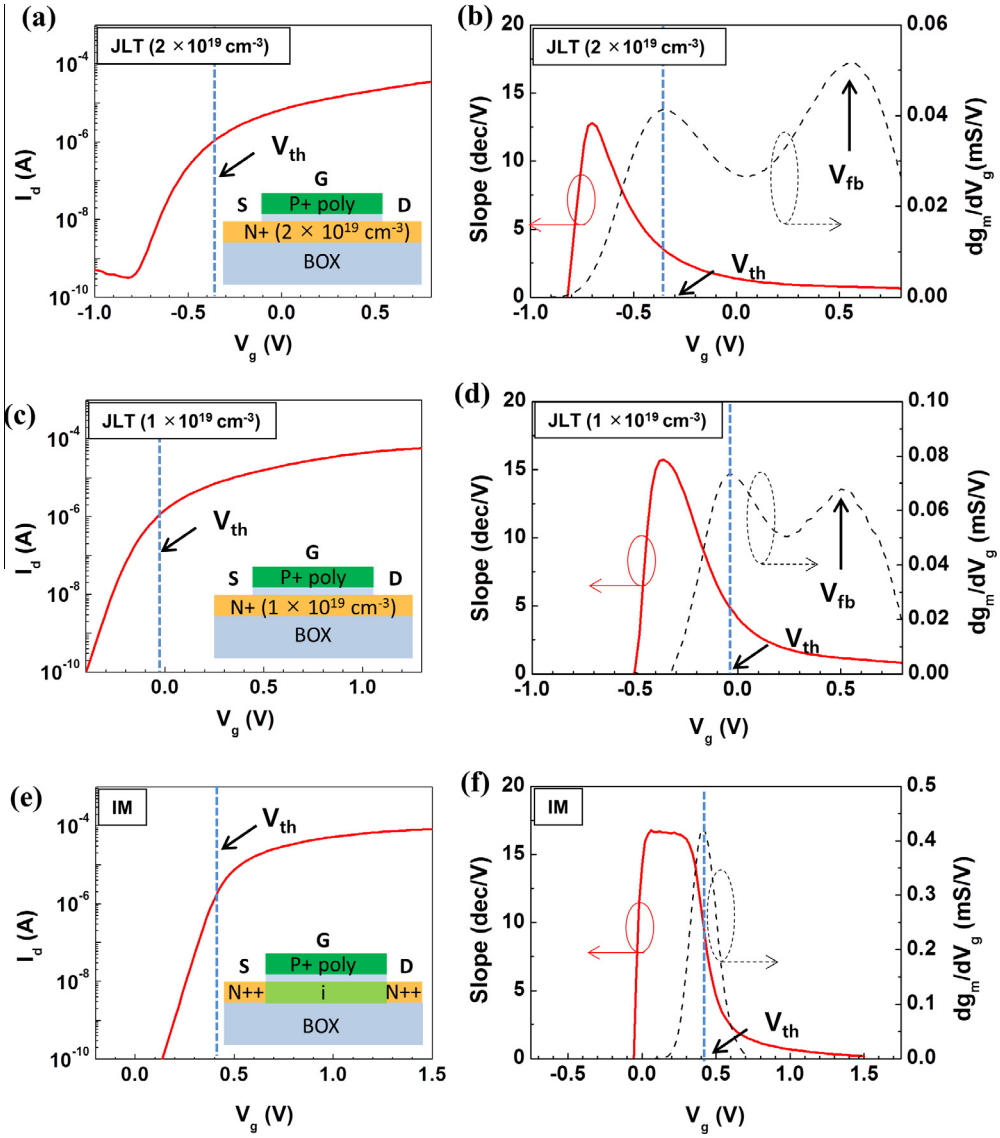

Fig. 1. The transfer curve at room temperature, the derivative of transconductance (dg_m/dV_g) and the slope (dLog(I_d)/dV_g) for junctionless transistors (JLT) with different doping concentration and the inversion-mode transistor (W_M = 10 μm, L_M = 1 μm). Insets are schematics for each device. Interestingly, both JLTs show a peak point with very narrow flat region (~20 mV) on the slope in subthreshold regime while IM transistor exhibits clearly a flat slope region (~230 mV).