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Determining the base resistance of InP HBTs: An evaluation of methods and structures

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ABSTRACT

Many different methods can be found in the literature for determining both the internal and external base series resistance based on single transistor terminal characteristics. Those methods are not equally reliable or applicable for all technologies, device sizes and speeds. In this review, the most common methods are evaluated regarding their suitability for InP heterojunction bipolar transistors (HBTs) based on both measured and simulated data. Using data generated by a sophisticated physics-based compact model allows an evaluation of the extraction method precision by comparing the extracted parameter value to its known value. Based on these simulations, this study provides insight into the limitations of the applied methods, causes for errors and possible error mitigation. In addition to extraction methods based on just transistor terminal characteristics, test structures for separately determining the components of the base resistance from sheet and specific contact resistances are discussed and applied to serve as reference for the experimental evaluation.

1. Introduction

InP HBTs are among the fastest transistors that have been fabricated [1]. They retain a comparatively high breakdown voltage even at high speed, making them ideal candidates for ultra-high-speed communication circuits and systems. Recent integration efforts of InP and other III–V materials on silicon CMOS [2], making use of the advantages of both technologies, may enable a more widespread deployment of InP devices in the future.

In order to design and optimize circuits that exploit the peak performance of a given HBT technology, physics-based geometry scalable compact models are required due to their predictive capability. For instance, their parameters can be determined at relatively low frequencies while retaining accuracy up to frequencies where experimental characterization is difficult for small-signal and impossible for large-signal operation [3]. Such compact models are not commonly used for InP HBTs, in part due to the difficulty posed by accurate parameter extraction. Modern compact models can have upwards of 100 parameters, many of which describe physical effects that cannot easily be separated, but may have different frequency or temperature dependencies. When trying to determine model parameters by curve fitting, this complexity usually leads to a bad agreement between model and measurement beyond the range of the available fit data if a result is obtained at all. A unique and reliable determination of parameters simplifies the extraction effort greatly and increases the reliability of compact models [4,5]. This study aims, in part, at improving the overall compact model quality for InP HBTs.

The base series resistance R_B impacts the high-frequency behavior of HBTs as well as its DC characteristics due to the voltage drop caused by the base current. This is especially true for InP HBTs due to the much lower DC current gain compared to, e.g., SiGe HBTs. The impact of R_B is expected to increase with advancing technology nodes due to shrinking vertical dimensions and correspondingly higher contact and partially also sheet resistances [6,7]. A large number of methods exist in the literature for the determination of R_B [8–25] with, unfortunately, widely varying results when applied to the same transistor (e.g. [5,8]). The list gathered in this paper corresponds to a careful selection of the most promising extraction methods, which have been applied in this study to the devices from different geometries and technologies described in Section 2.

Typically, in the literature verification of an extraction method is attempted by comparing its results to another method or by adding a known resistance. This still leaves the question open how accurate either of the methods actually is. Therefore, in order to be able to evaluate the absolute (achievable) accuracy, in this study

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the extraction methods under investigation will be applied to simulation data generated by the physics-based compact model HICUM [26], which has been shown to accurately model InP DHBTs [27]. The advantages of this approach are:

- The target value (in this case for R_B) is known so that the error of a method can be easily assessed, and
- the compact model allows the analysis of the limitations of a method by turning physical effects on or off and providing access to internal nodes and element values.

The effectiveness of this method has already been shown for other parameters [28–30]. As a necessary precondition, the model needs to include all relevant physical effects and to accurately reproduce the measured data in the region of interest. A potential problem of this approach is the mapping of the distributed nature of the base resistance into a lumped element. However, given that extraction methods assume lumped element equivalent circuits, applying them to compact model data represents a best-case scenario. Additionally, emitter current crowding, emitter perimeter injection and the split of R_B into its external and internal component are taken into account in HICUM. An alternative to extraction methods based directly on terminal characteristics of a single transistor is the use of special test structures combined with knowledge about the transistor geometry. Such structures, including the tetrode [31,32], have been used for SiGe HBTs since at least the seventies, and the geometry dependence of the base resistance has been well known [33–35]. Corresponding results are also presented in this work.

This paper is organized as follows: in Section 2, the investigated technologies are briefly described. Section 3 summarizes the essential features of the applied extraction methods and discusses their error sources. The results of the extraction methods are presented in Section 4. Section 5 presents the special test structures, associated extraction method and experimental results. Comparisons with measurements are shown in Section 6. Summarizing conclusions are given Section 7.

2. Investigated process technologies

A variety of InP HBT process technologies have been investigated. For each process, several devices were measured which differed in emitter mesa width (b_{E0}), length (l_{E0}) and area ($A_{E0} = b_{E0} * l_{E0}$). The investigated transistors are from a GCS process [36] with $A_{E0} = \mathbf{0.8} \times (\mathbf{3}, \mathbf{5}, \mathbf{10})\ \mu m^2$ as well as $A_{E0} = (\mathbf{0.5}, \mathbf{0.8}, \mathbf{1}, \mathbf{1.5}, \mathbf{2}) \times 15\ \mu m^2$ from two different process runs, both with $(f_T, f_{max}) = (300, 250)$ GHz, a Teledyne process [37] with $A_{E0} = 0.5 \times (3, 5, \mathbf{10})\ \mu m^2$ and $(f_T, f_{max}) = (300, 450)$ GHz and an FhG IAF process [38] with $A_{E0} = 0.7 \times (2, \mathbf{4}, 12)\ \mu m^2$ and $(f_T, f_{max}) = (300, 260)$ GHz. Dimensions marked in bold indicate transistor sizes for which a complete compact model was available. For the GCS transistors, both geometry scalable HICUM/L2 parameters were extracted using suitable test structures on a special test chip [27] and a HICUM/L0 model was created based on single-transistor extraction methods [39]. For the two other technologies, only HICUM/L0 model parameters could be determined since only single-transistor structures were available. The HICUM model has been in use in the industry for many years and is capable of accurately modeling all available device sizes.

All data for the R_B related investigation were generated and measured, respectively, at a chuck temperature of $T_0 = 300$K. All S-parameter data are open-short deembedded; parasitic capacitances as mentioned in this publication refer to the influence of vias and device contacts which cannot be deembedded in this fashion.

3. Extraction methods

The extraction of model parameters from terminal quantities (currents, voltages or small-signal parameters) usually assumes a simplified equivalent circuit compared to those provided in PDKs and used for circuit design (e.g. HICUM/L2). The simplification is necessary in order to derive sufficiently simple (i.e. explicit) expressions for the desired parameter. Fig. 1 shows the most sophisticated version of the DC and small-signal equivalent circuit employed in extraction methods along with the relevant circuit element names used in this paper. All results and discussions refer to vertical npn transistors but can also be applied to vertical pnp transistors.

In this investigation, methods known to possess a flawed physical background, such as the extraction of the base resistance from the collector current characteristic [9], have been omitted. The semi-insulating substrate of III–V technologies prevents the use of methods based on a substrate current flow [10]. Moreover, methods based on impact ionization (e.g. [11]) are unsuitable for III–V devices since the high breakdown voltage caused by the high-bandgap collector material in combination with high current densities leads to a high probability of device destruction when attempting to take the required measurements. Note that the associated elements have already been omitted from the equivalent circuit in Fig. 1. Most compact models differentiate between the bias-independent external part of the base resistance R_{Bx} and the internal, bias-dependent part R_{Bi} so that

$$R_B = R_{Bx} + R_{Bi}. \tag{1}$$

Typically, the two contributions are separated by extracting R_B for different bias points.

3.1. Extraction from the DC base resistance

This method was first presented in [12]. It assumes that any deviation of the base current from its ideal exponential characteristic is due to the voltage drop across the series resistances. Rearranging the base current equation yields

$$\frac{m_{BE} V_T}{I_C} \ln\left(\frac{I_{B0}}{I_B}\right) = \left(R_E + \frac{R_{Bi}}{B_f}\right) + \frac{R_E + R_{Bx}}{B_f}, \tag{2}$$

with the emitter series resistance R_E, the nonideality factor of the BE diode m_{BE}, which was added here compared to [12] and the forward DC current gain B_f. The resistances are extracted from a linear regression of the measured l.h.s. term w.r.t. $1/B_f$. Assuming R_E to be known, the external base resistance R_{Bx} can be determined from the slope and the internal base resistance R_{Bi} from the intercept with the y-axis since it is assumed in [12] that the term R_{Bi}/B_f is not bias-dependent.

The method suffers from various shortcomings. First, self-heating is neglected but occurs in the region with a measurable voltage drop across the series resistances. Second, an ideal I_B characteristic is assumed. This is a problem in InP HBTs since the base current is dominated by recombination rather than backinjection [40]. While it is possible and common, even in dedicated III–V compact models [41], to model it using traditional diode equations, a single ideal diode is usually not sufficient and the required ideal region for I_B is almost non-existent at medium and high forward bias. Third, the bias dependence of R_{Bi} does not cancel with that of $1/B_f$.

The combination of these effects makes the method very unreliable for InP HBTs. Fig. 2a shows the linear regression used for the extraction from (2), showing a negative slope and thus a negative extracted R_{Bx} as an example. The slope of $\ln(I_B)$ with V_{BE}, shown